

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG TELECOMMUNICATIONS
AMERICA GENERAL, L.L.C.,
SAMSUNG SEMICONDUCTOR, INC., and
SAMSUNG AUSTIN SEMICONDUCTOR L.L.C.,

Plaintiffs,

v.

ON SEMICONDUCTOR CORP. and
SEMICONDUCTOR COMPONENTS
INDUSTRIES, LLC,

Defendants.

Civil Action No. 06-720 (JJF)

ON SEMICONDUCTOR CORP. and
SEMICONDUCTOR COMPONENTS
INDUSTRIES, LLC,

Plaintiffs,

v.

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC.,
SAMSUNG TELECOMMUNICATIONS
AMERICA GENERAL, L.L.C.,
SAMSUNG SEMICONDUCTOR, INC., and
SAMSUNG AUSTIN SEMICONDUCTOR L.L.C.,

Defendants.

Civil Action No. 07-449 (JJF)

**SAMSUNG'S OPENING BRIEF IN SUPPORT
OF ITS PROPOSED CLAIM CONSTRUCTIONS**

YOUNG CONAWAY STARGATT &
TAYLOR, LLP

Josy W. Ingersoll (No. 1088)

John W. Shaw (No. 3362)

Andrew A. Lundgren (No. 4429)

The Brandywine Building

1000 West Street, 17th Floor

Wilmington, Delaware 19899-0391

302-571-6600

alundgren@ycst.com

*Attorneys for SAMSUNG ELECTRONICS CO.,
LTD., SAMSUNG ELECTRONICS AMERICA,
INC., SAMSUNG TELECOMMUNICATIONS
AMERICA GENERAL, L.L.C., SAMSUNG
SEMICONDUCTOR, INC., and SAMSUNG
AUSTIN SEMICONDUCTOR, L.L.C.*

OF COUNSEL:

John M. Desmarais

Jon T. Hohenthauer

James E. Marina

KIRKLAND & ELLIS LLP

153 East 53rd Street

New York, NY 10022-4611

212-446-4800

jdesmarais@kirkland.com

jhohenthauer@kirkland.com

jmarina@kirkland.com

Edward C. Donovan

KIRKLAND & ELLIS LLP

655 Fifteenth Street, N.W.

Washington, D.C. 20005-5793

202-879-5000

edonovan@kirkland.com

Dated: April 14, 2008

EXHIBIT LIST

The following exhibits cited herein refer to the exhibits to the Declaration Of Brian Lee In Support Of Samsung's Proposed Claim Constructions, filed concurrently herewith.

- Exhibit A:*** U.S. Patent No. 5,000,827
- Exhibit B:*** U.S. Patent No. 5,000,827 File History
- Exhibit C:*** U.S. Patent No. 5,361,001
- Exhibit D:*** U.S. Patent No. 5,361,001 File History
- Exhibit E:*** U.S. Patent No. 5,563,594
- Exhibit F:*** U.S. Patent No. 5,563,594 File History
- Exhibit G:*** U.S. Patent No. 6,362,644
- Exhibit H:*** U.S. Patent No. 6,362,644 File History
- Exhibit I:*** U.S. Patent No. 5,252,177
- Exhibit J:*** U.S. Patent No. 5,252,177 File History
- Exhibit K:*** ALEXANDER WATT & ARNOLD PHILIP, THE ELECTRO-PLATING AND ELECTRO-REFINING OF METALS (1902)
- Exhibit L:*** U.S. Patent No. 4,170,959
- Exhibit M:*** U.S. Patent No. 4,906,341
- Exhibit N:*** MODERN DICTIONARY OF ELECTRONICS (6th ed. 1984)
- Exhibit O:*** DICTIONARY OF ELECTRONIC PACKAGING, MICROELECTRONIC, & INTERCONNECTION TERMS (1990)
- Exhibit P:*** MCGRAW-HILL ELECTRONICS DICTIONARY (5th ed. 1994)
- Exhibit Q:*** ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY (1992)
- Exhibit R:*** MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS (5th ed. 1994)
- Exhibit S:*** THE ILLUSTRATED DICTIONARY OF ELECTRONICS (6th ed. 1994)
- Exhibit T:*** PAUL HOROWITZ & WINFIELD HILL, THE ART OF ELECTRONICS (2d ed. 1989)
- Exhibit U:*** U.S. Patent No. 5,228,052

- Exhibit V:*** PETER VAN ZANT, MICROCHIP FABRICATION, A PRACTICAL GUIDE TO SEMICONDUCTOR PROCESSING (2d ed. 1990)
- Exhibit W:*** COMPREHENSIVE DICTIONARY OF ELECTRICAL ENGINEERING (1999)
- Exhibit X:*** ON Semiconductor Corp. and Semiconductor Components Industries, L.L.C.'s Preliminary Proposed Claim Constructions served on March 17, 2008
- Exhibit Y:*** M. E. Burba et al., *Selective Dry Etching of Tungsten for VLSI Metallization*, 133 J. Electrochem. Soc., October 1986, at 2113.
- Exhibit Z:*** WEBSTER'S THIRD NEW INTERNATIONAL DICTIONARY (1986)
- Exhibit AA:*** WEBSTER'S NINTH NEW COLLEGIATE DICTIONARY (1988)
- Exhibit BB:*** MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS (4th ed. 1989).

– *Emphasis Added Unless Otherwise Noted* –

TABLE OF CONTENTS

	<u>Page</u>
INTRODUCTION	1
APPLICABLE LAW	1
ARGUMENT	4
I. U.S. PATENT NO. 5,000,827	4
A. Background Of The '827 Patent Technology	4
B. Proper Construction Of The Disputed Terms Of The '827 Patent	6
1. “metallized bumps”	6
2. “said bumps being of substantially uniform height across said substrate”	9
3. “altering the flow rate of said solution through said opening”	10
II. U.S. PATENT NO. 5,361,001	12
A. Background Of The '001 Patent Technology	12
B. Proper Construction Of The Disputed Terms Of The '001 Patent	13
1. “analog trimming”	13
2. “control signal”	16
3. “fixed value” and “setting said control signal to a fixed value”	17
III. U.S. PATENT NO. 5,563,594	19
A. Background Of The '594 Patent Technology	19
B. Proper Construction Of The Disputed Terms Of The '594 Patent	21
1. “a register having an input coupled for receiving parallel input data and having an output”	21
2. “a multiplexer having an input coupled to said output of said register for providing serial data”	22
3. “coupled”	24

4.	“comparator”	26
5.	“control signal”	28
6.	“first and second control signals match”	29
7.	“clock signal”	30
8.	“transfer data signal”	31
IV.	U.S. PATENT NO. 6,362,644	33
A.	Background Of The '644 Patent Technology	33
B.	Proper Construction Of The Disputed Terms Of The '644 Patent	35
1.	“termination signal” (claim 6) and “programmable termination” (claim 12).....	35
2.	“third and fourth pins for respectively receiving first and second termination signals” (claim 6) and “first and second load elements are coupled to third and fourth pins of the semiconductor package to provide a programmable termination” (claim 12).....	38
3.	“pin”	42
4.	“coupled”	44
5.	“terminate” (claim 6) and “loading” (claim 12)	46
6.	“load element”	48
V.	U.S. PATENT NO. 5,252,177	49
A.	Background Of The '177 Patent Technology	50
B.	Proper Construction Of The Disputed Terms Of The '177 Patent	52
1.	“photoresist pattern”	52
2.	“expose a top surface of said first conductive layer”	53
3.	“removing said photoresist pattern positioned on said insulation layer by plasma etching simultaneously forming a protective oxide layer” (claim 1) and “removing remaining photoresist positioned on said insulation layer by plasma ashing to simultaneously form a protective oxide	

	layer on said exposed top surface of said first conductive layer" (claim 8)	54
4.	"plasma etching" and "plasma ashing"	55
5.	"simultaneously form[ing] a protective oxide layer" and "simultaneously form[ing]"	57
6.	"protective oxide layer"	58
7.	"exposed top surface"	59
8.	"removing said oxide layer before forming a second conductive layer on said exposed top surface of said first conductive layer" (claim 1) and "removing said oxide layer before forming said second conductive layer on said exposed top surface of said first conductive layer" (claim 8)	59
CONCLUSION		60

TABLE OF AUTHORITIES**Page(s)****Cases**

<i>Abbott Labs. v. Andrx Pharms., Inc.</i> , 452 F.3d 1331 (Fed. Cir. 2006)	37, 48
<i>Agere Sys., Inc. v. Atmel Corp.</i> , 2004 WL 945162 (E.D. Pa. Apr. 30, 2004)	56
<i>Alloc v. Int'l Trade Comm'n</i> , 342 F.3d 1361 (Fed. Cir. 2003)	42
<i>Alpex Computer Corp. v. Nintendo Co.</i> , 102 F.3d 1214 (Fed. Cir. 1997)	3
<i>Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp.</i> , 55 F.3d 615 (Fed. Cir. 1995)	7
<i>Biotec Biologische Naturverpackungen GmbH v. Biocorp, Inc.</i> , 249 F.3d 1341 (Fed. Cir. 2001)	49
<i>Boehringer Ingelheim Vetmedica v. Schering-Plough</i> , 320 F.3d 1339 (Fed. Cir. 2003)	15
<i>Boston Scientific SciMed, Inc. v. EV3 Inc.</i> , 502 F. Supp.2d 931 (D. Minn. 2007)	26, 46
<i>C.R. Bard, Inc. v. U.S. Surgical Corp.</i> , 388 F.3d 858 (Fed. Cir. 2004)	3
<i>Catalina Mktg. Int'l, Inc. v. CoolSavings.com, Inc.</i> , 289 F.3d 801 (Fed. Cir. 2002)	6, 7, 9
<i>CCS Fitness, Inc. v. Brunswick Corp.</i> , 288 F.3d 1359 (Fed. Cir. 2002)	3
<i>Computer Docking Station Corp. v. Dell, Inc.</i> , Nos. 2007-1169 and 2007-1316, __ F.3d __, 2008 WL 752675 (Fed. Cir. Mar. 21, 2008)	41
<i>Conoco, Inc. v. Energy & Envtl. Int'l, L.C.</i> , 460 F.3d 1349 (Fed. Cir. 2006)	55, 60
<i>Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.</i> , 868 F.2d 1251 (Fed. Cir. 1989)	15
<i>Cultor Corp. v. A.E. Staley Mfg. Co.</i> , 224 F.3d 1328 (Fed. Cir. 2000)	3
<i>Ekchian v. Home Depot, Inc.</i> , 104 F.3d 1299 (Fed. Cir. 1997)	42
<i>Gen. Elec. Co. v. Nintendo Co.</i> , 179 F.3d 1350 (Fed. Cir. 1999)	16
<i>Hockerson-Halberstadt, Inc. v. Avia Group Int'l, Inc.</i> , 222 F.3d 951 (Fed. Cir. 2000)	41
<i>Innogenetics v. Abbott Labs.</i> , 512 F.3d 1363 (Fed. Cir. 2008)	8
<i>Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.</i> , 381 F.3d 1111 (Fed. Cir. 2004)	2
<i>Key Pharms. v. Hercon Labs. Corp.</i> , 161 F.3d 709 (Fed. Cir. 1998)	3

<i>Liebel-Flarsheim Co. v. Medrad, Inc.</i> , 358 F.3d 898 (Fed. Cir. 2004).....	53
<i>Markman v. Westview Instruments, Inc.</i> , 52 F.3d 967 (Fed. Cir. 1995), <i>aff'd</i> , 517 U.S. 370 (1996).....	2
<i>Microsoft Corp. v. Multi-Tech Sys., Inc.</i> , 357 F.3d 1340 (Fed. Cir. 2004).....	42
<i>O.I. Corp. v. Tekmar Co.</i> , 115 F.3d 1576 (Fed. Cir. 1997)	3
<i>On Demand Mach. Corp. v. Ingram Indus., Inc.</i> , 442 F.3d 1331 (Fed. Cir. 2006)	15
<i>PCTEL, Inc. v. Agere Sys., Inc.</i> , No. C03-02474 MJJ, 2006 WL 734385 (N.D. Cal. Mar. 20, 2006)	26, 46
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (en banc)	passim
<i>Poly-Am., L.P. v. GSE Lining Tech., Inc.</i> , 383 F.3d 1303 (Fed. Cir. 2004)	15
<i>Renishaw PLC v. Marposs Societa' per Azioni</i> , 158 F.3d 1243 (Fed. Cir. 1998)	2
<i>Spectrum Int'l v. Sterilite Corp.</i> , 164 F.3d 1372 (Fed. Cir. 1998).....	3
<i>Tate Access Floors, Inc. v. Maxcess Techs., Inc.</i> , 222 F.3d 958 (Fed. Cir. 2000).....	37, 48
<i>U.S. Surgical Corp. v. Ethicon, Inc.</i> , 103 F.3d 1554 (Fed. Cir. 1997).....	25, 44, 49
<i>Vitronics Corp. v. Conceptronic, Inc.</i> , 90 F.3d 1576 (Fed. Cir. 1996).....	2, 3

Plaintiffs Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Telecommunications America General, L.L.C., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, L.L.C. (collectively, “Samsung”) respectfully submit this brief in support of their proposed constructions for the disputed claim terms of the five patents-in-suit.

INTRODUCTION

Samsung filed this patent infringement action against ON Semiconductor Corp. and Semiconductor Components Industries, LLC (collectively, “Defendants”) on November 30, 2006. As part of this action, Defendants assert four patents against Samsung—U.S. Patent Nos. 5,000,827 (“the ’827 patent”), 5,361,001 (“the ’001 patent”), 5,563,594 (“the ’594 patent”), and 6,362,644 (“the ’644 patent”)—and Samsung asserts one patent against Defendants—U.S. Patent No. 5,252,177 (“the ’177 patent”). The claim construction hearing is set for May 21, 2008.

Samsung’s proposed claim constructions addressed herein are based upon the intrinsic record of each of the patents-in-suit, including the claims, specifications, and prosecution histories, and the ordinary and customary meaning of the terms to those skilled in the art. Samsung’s constructions are intended to explain, in a simple manner, the disputed terms to facilitate resolution of the issues. In contrast, Defendants seek to depart from the intrinsic record and the ordinary and customary meaning of the terms in an effort to capture technologies far outside the scope of the alleged inventions described in their own patents, while at the same time improperly reading numerous limitations into the otherwise plain language of Samsung’s patent. For the reasons set forth herein, Samsung respectfully requests that the Court adopt Samsung’s proposed constructions for each of the five patents-in-suit.

APPLICABLE LAW

It is the court’s “power and obligation to construe as a matter of law the meaning of language used in the patent claim.” *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979

(Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996). As a starting point, a claim term is given the “ordinary and customary” meaning it would have had to a person of ordinary skill in the art at the time of the invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (*en banc*). For some terms, that meaning may be readily apparent so that construction “involves little more than the application of the widely accepted meaning of commonly understood words.” *Id.* at 1314. General purpose dictionaries may be helpful in such circumstances. *Id.*

“Because the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to ‘those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean.’” *Id.* (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004)). Those sources may include both intrinsic evidence (the claims, specification, and prosecution history) and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. *Phillips*, 415 F.3d at 1314; *Vitronics Corp. v. Conceptoronic, Inc.*, 90 F.3d 1576, 1582-83 (Fed. Cir. 1996).

Of those sources, the “intrinsic evidence is the most significant source of the legally operative meaning of disputed claim language.” *Vitronics*, 90 F.3d at 1582. In that regard, the claims do not stand alone, but must be read in view of the specification, of which they are a part. *Phillips*, 415 F.3d at 1315. Accordingly, “the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent’s description of the invention will be, in the end, the correct construction.” *Id.* at 1316 (quoting *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)). For example, the intrinsic evidence may reveal that the patentee

acted as its own lexicographer and defined a claim term, in which case that definition governs. *See id.*; *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002).

The intrinsic evidence may also reveal a disclaimer or disavowal of claim scope which, if present, is dispositive. *Phillips*, 415 F.3d at 1316. For example, arguments to the Patent Office during prosecution distinguishing the invention from the prior art function as a disclaimer for claim construction purposes. *Spectrum Int'l v. Sterilite Corp.*, 164 F.3d 1372, 1379 (Fed. Cir. 1998); *Alpex Computer Corp. v. Nintendo Co.*, 102 F.3d 1214, 1220-22 (Fed. Cir. 1997). In that regard, “[b]y distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover.” *Spectrum*, 164 F.3d at 1378-79; *see also O.I. Corp. v. Tekmar Co.*, 115 F.3d 1576, 1581 (Fed. Cir. 1997) (holding that “passages” were non-smooth where “the description expressly distinguishes over [smooth] prior art ‘passages’”). Accordingly, a claim cannot be “correctly construed to cover what was expressly disclaimed.” *Cultor Corp. v. A.E. Staley Mfg. Co.*, 224 F.3d 1328, 1331 (Fed. Cir. 2000).

Extrinsic evidence may also be considered, but “while extrinsic evidence ‘can shed useful light on the relevant art,’ we have explained that it is ‘less significant than the intrinsic record in determining ‘the legally operative meaning of claim language.’” *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)). Among the available sources of extrinsic evidence, dictionaries and technical treatises are often consulted because they can provide accepted meanings of terms not biased by litigation. *See, e.g., id.*; *Vitronics*, 90 F.3d at 1584 n.6. Expert testimony may also be considered provided that it is supported by evidence, not conclusory, and not at odds with the intrinsic record. *Phillips*, 415 F.3d at 1318; *Key Pharms. v. Hercon Labs. Corp.*, 161 F.3d 709, 716 (Fed. Cir. 1998).

ARGUMENT

I. U.S. PATENT NO. 5,000,827

Defendants' '827 patent is directed to a method of forming "metallized bumps" on a flat substrate, like a semiconductor wafer, using an electroplating technique. (Ex. A at 3:9-13.)¹ According to the '827 patent, the "bumps" formed by this method have a more uniform height than those formed by the prior art electroplating methods. (Ex. A at 5:60-6:3.) There are only two claims in the patent, and only three disputed terms.

A. Background Of The '827 Patent Technology

Electroplating is a well known way of depositing metal onto a flat substrate that was first developed in the 1800s. (Ex. K, THE ELECTRO-PLATING AND ELECTRO-REFINING OF METALS.) At a basic level, a substrate to be plated is placed in contact with a solution containing metallic compounds of, for example, silver or tin. When a voltage is applied to the plating apparatus, the metal ions in the solution flow to the substrate surface to form a layer of metal. A prior art electroplating apparatus is shown in Fig. 5 of the '827 patent. (Ex. A at Fig. 5.)

Electroplating has long been used in the semiconductor industry as one way of depositing metal onto the semiconductor wafer. (*See, e.g.*, Ex. L at 1:7-10, 1:22-30.) As explained by the '827 patent, one prior art way that electroplating is used in the semiconductor industry is to form electrical contacts on the semiconductor substrate in the form of metallic bumps. (Ex. A at 1:66-68.) Electrical contacts are necessary for making the electrical connections that allow an integrated circuit to work within a larger electronic system, such as a computer. Bumps are one type of electrical contacts used by semiconductors, and electroplating is one way of making such

¹ Patent citations in the format #:# to refer to the applicable column:line number(s).

bumps. (*See, e.g.*, Ex. M at 1:52-55.) In Figures 3A-C, the '827 patent depicts the steps used in "plating of a metallization bump onto a terminal area." (Ex. A at 3:63-65, Figs. 3A-C.)

The alleged invention of the '827 patent is a method of forming "bumps" or contacts having a substantially uniform height. (Ex. A at 1:9-13.) Figure 6 is described as showing non-uniform bump heights obtained using the prior art device of Figure 5. (Ex. A at 4:4-6, Fig. 6.) The '827 patent also discloses a different prior art apparatus for electroplating bumps onto a substrate called a "cup plating" apparatus. (Ex. A at 5:1-2.) Figures 9 and 10 are described as showing "uniform" bump heights resulting from the use of the alleged inventive method with a cup plating apparatus. (Ex. A at 4:14-19, Figs. 9-10.)

The claimed invention purports to overcome a well known problem in the art—the "edge effect"—that causes uneven bump heights across a wafer when using a cup plating apparatus. (Ex. A at 2:59-62, 3:3-8, 5:1-6, Fig. 6; *see also* Ex. L at 1:22-30.) According to the '827 patent, the "edge effect" causes bumps on the edge of the substrate to be higher than those in the middle when using a cup plating apparatus. (Ex. A at 5:1-2.) The '827 patent inventors purported to overcome this "edge effect" by "selectively altering the metallic ion concentration of the electroplating solution near the edge(s) of the wafer substrate." (Ex. A at 2:59-62.) In particular, the inventors alleged to overcome the edge effect by altering three process parameters affecting the ion concentration: the diameter of the "cup" that contains the solution, the distance of the wafer from the cup, and the flow rate of the solution over the wafer. (Ex. A at 2:63-3:8.)

During prosecution, the '827 patent applicants sought to obtain patent coverage on a method of forming metallic bumps by simply "altering the metallic concentration of said electroplating solution in a predetermined area." (Ex. B at B-28.) Those claims were rejected based on prior art cup plating patents cited by the Patent Office. (Ex. B at B-63.) Indeed, the '827 applicants acknowledged that this prior art showed several examples of "electroplating

apparatus similar to that used by applicants.” (Ex. B at B-71.) Moreover, the applicants acknowledged that at least one of the cited prior art references “teaches providing uniform height of electrodeposition across the surface of the substrate.” (*Id.*) As a result, the ’827 applicants were forced to further limit application claim 1 to require that “**all** of the [] altering steps [cup size, height, and flow rate] are used to control the concentration.” (Ex. B at B-70.) Claim 1 now recites that the ion concentration used in the method must be altered by all three of these parameters. (Ex. A at claim 1, 6:56-62.)

B. Proper Construction Of The Disputed Terms Of The ’827 Patent

1. “metallized bumps”

Samsung’s Construction	Defendants’ Construction
“Small mounds of metal on a semiconductor pad that are utilized as contacts.” The preamble is a limitation.	ON Semiconductor notes that this term appears only in the preamble of the asserted claim. Because this term does not recite limitations or give life, meaning, and vitality to the claim, no construction is needed. If the Court is inclined to construe this term, however, ON Semiconductor contends that it should be construed as follows: “the non-planar accumulation of a metal layer or layers.”

There are two general disputed issues regarding the term “metallized bumps”: (1) whether it limits the claim; and (2) what it means. The term plainly is a claim limitation. *First*, the term appears not only in the preamble, but also twice more in the body of the claim to further limit the recited process, including the limitations that require “permit[ting] the growth of said metallization bumps” and “controlling the growth of said metallization bumps.” (Ex. A at claim 1, 6:41-48.) Thus, the term as it appears in the preamble is the only antecedent for its later use in the body of the claim, and is used in the body of the claim to expressly limit the claim scope. *See Catalina Mktg. Int’l, Inc. v. CoolSavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (explaining preamble may limit claim where there is “dependence on a particular disputed preamble phrase for antecedent basis” or when “the preamble is essential to understand

limitations or terms in the claim body”). Moreover, dependent claim 2 further limits the recited “metallized bumps” in the preamble of claim 1 to a particular selection of materials. (Ex. A at claim 2, 6:63-65.) Dependent claim 2 would be indefinite if the preamble was not a limitation. Accordingly, the preamble limits the claim by reciting terms later recited as limitations within the body of the claim. *See Bell Commc’ns Research, Inc. v. Vitalink Commc’ns Corp.*, 55 F.3d 615, 621 (Fed. Cir. 1995) (holding that the preamble in a method claim was a limitation where terms from the preamble were further referenced in the body of the claim). *Second*, the application shows that where the applicants sought to obtain a method claim not limited to forming bumps, they knew how to do so. (Ex. B at B-35-36.) The Patent Office rejected these claims in view of the prior art, however, and the ’827 applicants abandoned any effort to obtain such coverage. (Ex. B at B-63, B-70.) For this additional reason, the term “metallized bumps” in the preamble must be construed as a limitation. *See Catalina*, 289 F.3d at 808.

The meaning of “metallized bumps” is similarly straightforward. A “bump” in the semiconductor industry means a small mound formed of metal on a semiconductor pad that is utilized as a contact. (See Ex. N, MODERN DICTIONARY OF ELECTRONICS at 121 (bump: “A means of providing connections to terminal areas of a device. A small mound is formed on the device (or substrate) pads, and is utilized as a contact for face-down bonding.”).) That is the ordinary meaning to those skilled in the art and the only meaning used for the term in the ’827 patent specification. (See *id.*; see also, e.g., Ex. A at 1:9-13 (“metallization bumps on terminal areas of electrical circuits”), 3:31-34, 4:28-31.) Indeed, in every instance the term is used in the specification, it is used as a type of contact—not any random accumulation of material above the plane of the substrate. (See, e.g., Ex. A at 1:9-13, 3:31-34, 4:28-31.)

Likewise, the only use of “bump” in the prosecution history and cited prior art is the term’s understood meaning to those skilled in the semiconductor manufacturing art as referring

to a type of contact. (*See, e.g.*, Ex. B at B-28 (“metallization bumps predetermined on terminal areas”), B-70 (“[C]laim 7, specifically recites that the metallization bumps of claim 6 are comprised of metal selected from the group consisting of silver and tin.”), B-86-87 (describing the “external electrode 8a”), B-93 at Fig. 9 (illustrating the “external electrode 8a” as a bump).) And the extrinsic evidence shows those skilled in the art understood and used the term “bump” exactly as the ’827 patent specification does to refer to a type of electrical contact made from a mound of material. (*See, e.g.*, Ex. N, MODERN DICTIONARY OF ELECTRONICS at 121; Ex. O, DICTIONARY OF ELECTRONIC PACKAGING, MICROELECTRONIC, & INTERCONNECTION TERMS at 16 (bump: “A small mound or hump that is formed on the chip or the substrate bonding pad and is used as a contact in facedown bonding.”).)

Defendants’ proposed construction, based on an abstract dictionary definition, is at odds with the term’s ordinary meaning, and the term’s use in the intrinsic evidence. In the semiconductor manufacturing field, a “metallized bump” does not refer to a *shape*—as Defendants contend—but rather *a thing, i.e.*, a contact. (*See id.*) And, to the extent that the context of the use of the term “metallized bumps” is not already clear from the patent, the “metallized bumps” in the ’827 patent are described and claimed as being in “predetermined terminal areas,” *i.e.*, where the electrical connections are to be made. (Ex. A at 1:9-13 (“metallization bumps on terminal areas of electrical circuits”), 3:31-34, 4:28-31.) At bottom, Defendants’ reliance on an abstract dictionary definition improperly takes the limitation out of the context of the patent—“the very error of construction that [the Federal Circuit] warned against in *Phillips*.” *See Innogenetics v. Abbott Labs.*, 512 F.3d 1363, 1371 (Fed. Cir. 2008) (*quoting Phillips*, 415 F.3d at 1321 (“The main problem with elevating the dictionary to such prominence is that it focuses the inquiry on the abstract meaning of words rather than on the meaning of claim limitations within the context of the patent.”))).

2. “said bumps being of substantially uniform height across said substrate”

Samsung's Construction	Defendants' Construction
“Small mounds of metal utilized as contacts having substantially the same height above the semiconductor pad on which they are formed across the wafer.” The preamble is a limitation.	ON Semiconductor notes that this phrase appears only in the preamble of the asserted claim. Because this term does not recite limitations or give life, meaning, and vitality to the claim, no construction is needed. However, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following construction: substantially uniform height: “approximately the same distance between the top of the bump and the top surface of the substrate.”

The disputes between the parties regarding this phrase in the preamble of claim 1 of the '827 patent mirror those described above with respect to “metallized bumps.” *First*, the parties dispute whether the preamble phrase is a limitation. For all the reasons described above with respect to the term “metallized bumps,” this phrase is a limitation on the method claim. Indeed, the entire point of the claimed method—and the '827 patent—is to form “bumps” of substantially the same height. (Ex. A at 3:9-13; claim 1, 6:30-33.) Defendants would nonetheless read this limitation out of the claim, rendering the recited method meaningless. Defendants' position asking the Court to ignore the very thing it told the Patent Office was inventive should be rejected. *See Catalina*, 289 F.3d at 808 (“[W]hen the preamble is essential to understand limitations or terms in the claim body, the preamble limits claim scope.”).

Second, the parties dispute the meaning of the phrase, and again the disputes are centered on the term “metallized bumps” that is incorporated within the phrase. Samsung incorporates by reference its argument with respect to “metallized bumps” above. The balance of the phrase is unambiguous and requires no construction other than the context of the “bumps” with respect to the wafer. Defendants' proposed construction ignores the term “metallized bumps” and instead construes the phrase “substantially uniform height.” Even then, Defendants' construction of this phrase fails to define the subject of the phrase—the relative heights of the bumps. Rather,

Defendants define how to measure the height of a single bump. Accordingly, Defendants' construction should be rejected as ignoring the meaning of the phrase to be construed.

3. "altering the flow rate of said solution through said opening"

Samsung's Construction	Defendants' Construction
"Changing the volume of electroplating solution per unit of time through the opening of the solution container during the formation of the metallic bumps to control their growth in a predetermined region of the substrate."	"Changing the volume of electroplating solution per unit of time flowing out of the opening."

The only issue between the parties with respect to this disputed phrase is whether, in the context of the overall claim, the flow rate must be altered *during* the formation of metallized bumps, *i.e.*, to "control[] the growth of [the] metallization bumps." (Ex. A at claim 1, 6:46-50, 1:56-62.) Put another way, Defendants' proposed construction would apparently permit "changing the volume of electroplating solution" at some time before—not during—the formation of the bumps as claimed. Defendants' construction flies in the face of the plain language of the claims, the arguments it made to the Patent Office—and common sense—and thus should be rejected.

There is no dispute between the parties that the method of claim 1 requires "changing the volume of electroplating solution per unit of time [*i.e.*, the flow rate] flowing out of the opening." The plain language of the claim requires that this "change" in flow rate occur during the practice of the method. Claim 1 is a "method of forming metallized bumps." (Ex. A at claim 1, 6:30-33.) The claim requires the step of "exposing [the] substrate to [the] electroplating solution to permit the growth of said metallization bumps on said terminal areas" and "*controlling the growth of said metallization bumps* in a predetermined region of said substrate *by altering the metallic concentration of said electroplating solution* in said predetermined region." (Ex. A at claim 1, 6:41-48.) In other words, the claimed growth of the bumps is

controlled by *changing*—not maintaining—the metallic ion concentration of the solution. The claim further requires that the “metallic ion concentration of said electroplating solution is *changed* by: ... (k) in step (h) *altering the flow rate* of said solution through said opening.” (Ex. A at claim 1, 6:56-62.) Step (h) recites “providing an inlet within the container *for pumping said solution* into said container, said solution exiting said container through said opening.” (Ex. A at claim 1, 6:53-55.) Thus, the language of claim 1 expressly requires changing the flow rate of solution while pumping the solution in order to control the growth of the metallization bumps.

This construction—that the change in flow rate occurs *during* the pumping of the fluid to form the bumps—is what the ’827 patent applicants argued to the Patent Office as distinguishing their invention from the prior art cup plating apparatus. (Ex. B at B-71.) In particular, the applicants relied upon this limitation noting that “the present invention is a method of forming metallization, such as bumps, of substantially uniform height across a substrate *by changing the ion concentration of a flowing electroplating solution* in a predetermined region(s) of the substrate.” (*See id.*)

The specification is consistent with this construction. As an initial matter, the only description of the relevance of the flow rate is that “it was not found to be a critical parameter,” a very different position than that which the applicants took during prosecution to avoid the prior art plating apparatus. (*Compare* Ex. B at B-71 *with* Ex. A at 5:43-45.) But the specification does describe that the solution is pumped over the substrate in the plating machine, consistent with the claim requirement of changing the flow rate while pumping. (Ex. A at 2:63-66.) And the flow rate obviously cannot “alter” unless the pump is pumping. Accordingly, all of the intrinsic evidence supports Samsung’s construction, including the plain language of the claims.

II. U.S. PATENT NO. 5,361,001

Defendants' '001 patent is directed generally to analog trim circuits, and specifically to a process for previewing a trim before locking the trim in place. (Ex. C at 1:7-10.) Only independent claim 4 is asserted.

A. Background Of The '001 Patent Technology

"In manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled by the manufacturing process" so that "capacitors and resistors may have the wrong value." (Ex. C at 1:11-14.) Accordingly, a type of calibration referred to as "trimming" is used during the test process to adjust the values of those circuit components "as necessary for proper operation of the circuit." (Ex. C at 1:16-24.) The '001 patent describes various problems associated with prior art trimming techniques, including speed, expense, and discarded parts resulting from improper trimming. (Ex. C at 1:30-2:2.)

The '001 patent attempts to solve the identified problems by providing a mechanism for previewing various trimming options before permanently setting the trim. (Ex. C at 2:3-5, 4:31-47.) That is accomplished with a trim circuit in which conduction through one or more passive elements, such as resistors, can be temporarily enabled or disabled with data signals before permanently setting the trim. (Ex. C at Abstract.) For example, Fig. 1 shows a trim circuit in which the aggregate resistance value is determined by the values of resistors 12, 14, 16, and 18.

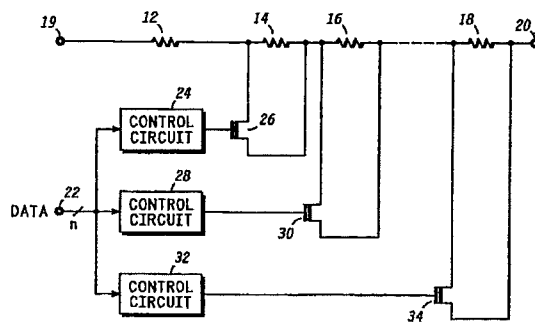


FIG. 1

↑
10

(Ex. C at 2:15-18, 2:37-45.) Resistors 14, 16, and 18 can be individually included or removed from the aggregate resistance value by activating or deactivating transistors 26, 30, and 34, in response to “control signals” from control circuits 24, 28, and 32. (Ex. C at 2:28-42, 3:29-4:2.)

During the preview step, the control signals are modified using input data signal 22 to determine the optimal combination of resistors to calibrate the circuit to the appropriate aggregate resistance value. (Ex. C at 3:29-4:2.) Once the optimal result is found, the control signals are fixed to permanently set the trim. (Ex. C at 4:7-17.) Accordingly, “[a] key feature of the present invention is to preview trimming at wafer test to provide an economical means of iteratively trimming....” (Ex. C at 4:31-33.)

B. Proper Construction Of The Disputed Terms Of The '001 Patent

1. “analog trimming”

Samsung's Construction	Defendants' Construction
“Making a fine adjustment of capacitance, inductance, or resistance of an analog circuit component.” The preamble is a limitation.	ON Semiconductor notes that this term appears only in the preamble of the asserted claim. Because this term does not recite limitations or give life, meaning, and vitality to the claim, no construction is needed. If the Court is inclined to construe this term, however, ON Semiconductor contends that it should be construed as follows: “modifying an analog value or quantity.”

The ordinary and customary meaning of “trim” or “trimming” is “making a fine adjustment of capacitance, inductance, or resistance of a circuit component”:

- **Trimming:** “*Fine adjustment* of capacitance, inductance, or resistance of a component during manufacture or after installation in a circuit.” (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 554.)
- **Trim:** “*to make a fine adjustment* of resistance, inductance, or capacitance in a circuit.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 2265.)
- **Trim:** “*Fine adjustment* of capacitance, inductance, or resistance of a component during manufacture or after installation in a circuit.” (Ex. R, MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS at 2070.)

- **Trim:** “*To make a fine adjustment*, as of a tuning control, balance control, output adjustment, or the like.” (Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 650.)

The term “trimming” does not, therefore, refer generically to modifying or changing a value, but rather, refers to making a *fine adjustment* to a circuit component.

The patent uses the phrase “analog trimming” in exactly the same way. For example, in the “Background of the Invention” section, the inventors explained that “analog trimming” is used to set proper circuit component values “[t]o compensate for the process variability” because “[i]n manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled” and therefore “capacitors and resistors may have the wrong value”:

In manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled by the manufacturing process as may be desired. For example, capacitors and resistors may have the wrong value, and MOS transistors may have the wrong gain setting. There are too many variables in the manufacturing process to yield absolute predictable results. Yet historically analog circuits often require very accurate voltage references, frequency references, and accurately ratioed elements.

To compensate for the process variability, many electronic circuits use analog trimming during test to set resistor values as necessary for proper operation of the circuit.

(Ex. C at 1:11-24; *see also id.* at 2:63-3:6.) Trimming is thus a mechanism for adjusting or calibrating circuit components to ensure that their values are within design parameters. Indeed, the entire patent is directed towards previewing adjustments to circuit component values during testing before permanently locking in those values. (Ex. C at 1:7-24, 1:39-2:5, 3:7-21, 3:49-54, 3:66-4:2, 4:7-17.) Notably, the inventor explained that “[a] *key feature of the present invention is to preview trimming at wafer test* to provide an economical means of iteratively trimming the resistive ladder using data provided by the tester.” (Ex. C at 4:31-34; *see also id.* at 4:34-51.)

Finally, the phrase “analog trimming” is a claim limitation that cannot be ignored—as advocated by Defendants—simply because it appears in the preamble. “In considering whether a preamble limits a claim, the preamble is analyzed to ascertain whether it states a necessary and defining aspect of the invention, or is simply an introduction to the general field of the claim.” *On Demand Mach. Corp. v. Ingram Indus., Inc.*, 442 F.3d 1331, 1343 (Fed. Cir. 2006). In that regard, “[t]he effect preamble language should be given can be resolved only on review of the entirety of the patent to gain an understanding of what the inventors actually invented and intended to encompass by the claim.” *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257 (Fed. Cir. 1989).

In light of the intrinsic record, it is clear that the phrase “analog trimming” is “not merely [a] circumstance[] in which the method may be useful, but instead [is] the *raison d’etre* of the claimed method itself,” as is “frequently” the case with method claims. *Boehringer Ingelheim Vetmedica v. Schering-Plough*, 320 F.3d 1339, 1345 (Fed. Cir. 2003). Indeed, the patent relates solely to the field of analog trimming—the patent title is “Circuit and Method of Previewing Analog Trimming,” the entire abstract of the invention relates to “[a]n analog trim circuit,” and the “Background of the Invention” states that the invention relates to analog trim circuits:

The present invention relates in general to analog trim circuits and, more particularly, to a technique of previewing the analog trim results before blowing a fuse to lock the trim in place.

(Ex. C at 1:6-10; *see also id.* at 4:31-32 (“A key feature of the present invention is to preview trimming....”).) The phrase “analog trimming” cannot, therefore, be disregarded as a claim limitation. *Poly-Am., L.P. v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004) (finding the preamble phrase “blown-film” is a limitation because “[t]he specification is replete with references to the invention as a ‘blown-film’ liner, including the title of the patent itself and the ‘Summary of the Invention,’” demonstrating “the inventor considered that the ‘blown-film’

preamble language represented an important characteristic of the claimed invention.”); *Gen. Elec. Co. v. Nintendo Co.*, 179 F.3d 1350, 1361-62 (Fed. Cir. 1999) (finding the preamble phrase “bit map display device” is a limitation because “[i]n light of the specification, to read the claim indiscriminately to cover all types of display systems would be divorced from reality.”). Accordingly, the phrase should be construed as set forth by Samsung above.

2. “control signal”

Samsung's Construction	Defendants' Construction
“A signal that enables or disables conduction through an associated passive element of a trim circuit.”	“A signal that conveys information about regulation or guidance.”

Beginning with the words of the claim, the “control signal” must enable and disable conduction through an associated passive element of the trim circuit:

4. A method of analog trimming, comprising the steps of:

enabling conduction through a passive element in response to a first state of a control signal;

disabling conduction through said passive element in response to a second state of said control signal;

activating said control signal in response to a data signal to enable and disable said conduction through said passive element, said activating step including the steps ...

(Ex. C at 5:27-6:2.) The phrase should be construed accordingly. *See Phillips*, 415 F.3d at 1314.

The specification uses the phrase “control signal” in exactly the same way. For example, as described in the specification and illustrated in Fig. 1, control circuits 24, 28, and 32 each supply a *control signal* to transistors 26, 30, and 34, respectively, thereby selectively enabling and disabling conduction through resistors 14, 16, and 18:

Control circuit 24 provides a control signal to the gate of MOS transistor 26. The drain and source of transistor 26 are coupled to first and second conduction terminals of resistor 14. Likewise, control circuit 28 provides a control signal to the gate of MOS transistor 30 which has its drain and source coupled across resistor 16. Control circuit 32 provides a control

signal to the gate of MOS transistor 34. The drain and source of transistor 34 are coupled across the first and second conduction terminals of resistor 18. The effective resistance through resistor ladder 10 is thus temporarily set by transistors 26, 30 and 34 *selectively enabling and disabling conduction through resistors 14-18 upon receiving a high state or low state of control signals* from control circuits 24, 28 and 32.

(Ex. C at 2:28-42.)

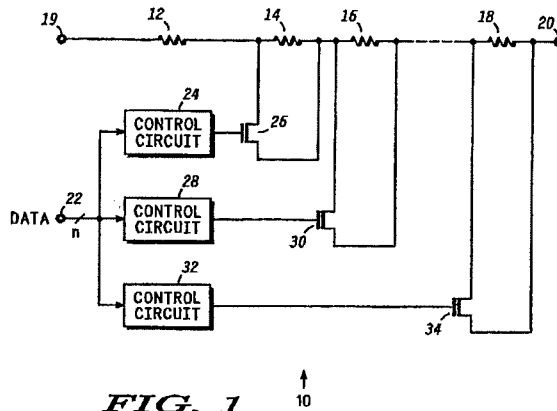


FIG. 1

The sole function of each “control signal” described and claimed in the ’001 patent is thus to enable or disable conduction through an associated passive element (resistors 14, 16, and 18) of the trim circuit. “Control signal” should therefore be construed as set forth by Samsung above.

3. “fixed value” and “setting said control signal to a fixed value”

Claim Term	Samsung’s Construction	Defendants’ Construction
“fixed value”	“A value that does not change.”	“A state that is not fluctuating or varying during a specified or predetermined time or condition.”
“setting said control signal to a fixed value”	“Permanently setting the state of the control signal.”	The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions: fixed value; control signal.

The ’001 patent is directed to a two step process: (i) *previewing* an analog trim; and then (ii) *permanently* setting the trim by blowing a fuse. (Ex. C at 1:7-10 (“The present invention relates in general to analog trim circuits and, more particularly, to a technique of previewing the analog trim results before blowing a fuse to lock the trim in place.”).)

Consistent with the claim language—“activating said control signal in response to a data signal to enable and disable said conduction through said passive element”—the specification explains that the previewing step is achieved by *temporarily* specifying trims with data signals:

- “*A key feature of the present invention is to preview trimming at wafer test to provide an economical means of iteratively trimming the resistive ladder using data provided by the tester. A data signal selectively trims the resistor ladder. The trimming is temporary and may be modified with different data signals to achieve optimal results.*” (Ex. C at 4:31-37.)
- “Note at this point, *the trimming process is temporary and dependent on the data signals* to control circuits 24, 28 and 32. No fuses have yet been blown to lock in the trim.” (Ex. C at 3:49-52.)
- “Again, *the trimming process is temporary and dependent on the data signals* to control circuits 24, 28 and 32. No fuses have yet been blown to lock in the trim.” (Ex. C at 3:66-4:1.)

The purpose of temporarily setting the trim is to preview various possible trims so that the optimal result may be selected. (Ex. C at 3:52-54 (“Thus, different combinations of resistors 14-18 may be previewed and checked to achieve optimal results.”); 4:1-2 (“Different combinations of resistors 14-18 may be tried and checked to achieve optimal results.”).)

After the previewing step is complete, the claim requires “setting said control signal to a fixed value after removal of said data signal.” (Ex. C at 6:6-7.) Consistent with the plain meaning of “setting ... to a fixed value,” the specification repeatedly and consistently explains that after removal of the data signal used in the preview step, the control signals are set to fixed values by blowing selected fuses, thereby *permanently* setting the trim:

- “*Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore the permanent trim. The control signals from control circuits 24, 28 and 32 are thus set to a fixed value by blowing the selected fuses 46 in the control circuits after removal of the data signal at terminal 22.*” (Ex. C at 4:10-17.)
- “[T]he fuse is severed and therefore *permanently* no longer conductive.” (Ex. C at 4:29-30.)

- “The laser trim system blows the appropriate fuses for each circuit under test according to the pattern previously determined by testing various trimming options. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore *sets the permanent trim.*” (Ex. C at 4:40-47.)
- “Hence, a need exists for an iterative trimming to evaluate the results of the test before *permanently setting the trim.*” (Ex. C at 2:3-5.)

The specification thereby expressly differentiates the preview step that involves *temporarily* setting a control signal value from the step of *permanently* setting a control signal value after the preview step is complete. Accordingly, consistent with the claims and specification, the terms should be construed as set forth by Samsung above.

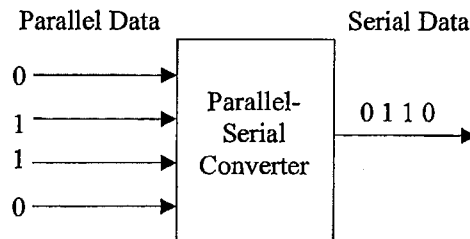
III. U.S. PATENT NO. 5,563,594

Defendants’ ’594 patent is directed to setting the proper timing for transferring data to and from a storage device, such as a register, in a parallel-serial or serial-parallel data converter. (Ex. E at Abstract, 1:7-22.) Only independent claim 8 is asserted.

A. Background Of The ’594 Patent Technology

“Parallel-serial converters are commonly used in digital circuit design to convert multi-bit signals to a string of data bits that are serially transmitted one at a time. Serial-parallel converters in turn convert the string of data bits back to multi-bit signals.” (Ex. E at 1:11-15.)

The figure below illustrates a block diagram of a simple parallel-serial conversion:



As illustrated, the converter receives four data input signals in parallel on separate input lines, each representing one “bit” of information such as a “1” or “0.” The parallel-serial converter converts those input signals into a single output signal that is transmitted serially, one bit at a

time. (Ex. E at 1:10-15; Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 1960 (serial data: “data that is transmitted sequentially, one bit at a time”).) The converter may be implemented with a device known as a “multiplexer,” which can select one of several inputs for output. (*Id.* at 1426; Ex. E at 2:15-17.)

Parallel-serial conversion takes time for an electrical circuit to process. One method of improving a circuit’s efficiency is to ensure that new information is available for processing immediately after the previously received information has been processed. (Ex. E at 1:23-59.) However, an external circuit providing parallel data to the converter may have difficulty determining exactly when new data should be provided, due in part to transmission delays between the circuits. (Ex. E at 1:23-56.) The ’594 patent purportedly solves this problem by enabling calibration of a circuit to account for different delays. (Ex. E at Abstract, 1:57-59.) Through experimentation, the proper delay is determined and the parallel-serial converter circuit is set to provide a “transfer data” signal to the external circuit at the appropriate time, thereby ensuing that new parallel data is available for processing immediately after the previously received data has been processed. (Ex. E at Abstract, 6:13-28.)

As illustrated below in Fig. 1 of the ’594 patent, the parallel-serial converter receives 32-bit parallel data through CMOS-ECL translator 12 and stores the parallel data in register 14. (Ex. E at 2:9-14.) Multiplexer 16 then converts that parallel data to serial data consisting of 32 sequential bits output on a single line. (Ex. E at 2:15-20.) At the appropriate stage of this parallel-serial conversion process, as determined by experimentation and configured by the “Octant Select” signal, phase delay logic 22 generates a “transfer data” signal requesting that the external circuit send the next set of parallel data so that it is available at register 14 immediately after the conversion of the previous set of parallel input data is complete. (Ex. E at Abstract, 3:13-30.)

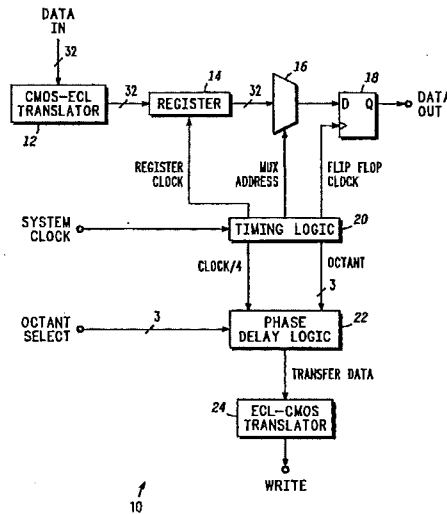


FIG. 1

The patent thus purportedly enables a circuit to be configured to achieve a maximum data transfer rate. (Ex. E at 3:24-30, 6:20-28.)

B. Proper Construction Of The Disputed Terms Of The '594 Patent

1. "a register having an input coupled for receiving parallel input data and having an output"

Samsung's Construction	Defendants' Construction
"A storage circuit that receives each bit of the input data simultaneously over several input lines."	It is ON Semiconductor's position that the Court need not construe this entire phrase. Instead, ON Semiconductor believes that the phrase can be understood according to the plain and ordinary meaning of its constituent terms or words. If the Court is inclined to construe this phrase, ON Semiconductor contends that it can be understood simply by construing the following terms: register: "a device capable of retaining or storing information."; coupled.

The ordinary and customary meaning of "register" is a storage circuit:

- **Register:** "A circuit that holds information in binary format to be processed or transferred." (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 448.)
- **Register:** "The computer hardware for storing one machine word." (Ex. R, MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS at 1678.)

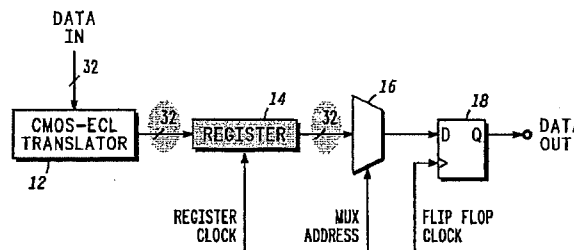
The claim language, however, further defines the structure of the claimed register—it must have an input coupled for receiving parallel input data and an output. Accordingly, the whole phrase

should be construed for proper context. *See Phillips*, 415 F.3d at 1314 (“To begin with, the context in which a term is used in the asserted claim can be highly instructive.”).

Considering the entire phrase, the ordinary and customary meaning of “parallel input data” is the simultaneous input of data through multiple wires:

- **Parallel input/output:** “the *simultaneous transmission of data* to and from a computer through multiple wires.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 1571.)
- **Parallel:** “Pertaining to the type of operation in a computer when *all elements in an information item (bits in a word, e.g.) are acted upon simultaneously rather than serially (one at a time).*” (Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 480.)
- **Parallel:** “*Simultaneous transmission* of, storage of, or logical operations on the parts of a word, character, or other subdivision of a word in a computer, using separate facilities for the various parts.” (Ex. R, MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS at 1443.)

Consistent with that ordinary and customary meaning, Fig. 1 (excerpted below) illustrates that 32 bits of parallel input data are input to (and then output from) register 14.



The specification describes the same thing. (Ex. E at 2:9-20.) Accordingly, the phrase should be construed as set forth by Samsung above.

2. “a multiplexer having an input coupled to said output of said register for providing serial data”

Samsung's Construction	Defendants' Construction
“A circuit that sequentially transmits the parallel input data from the register one bit at a time over a single output line.”	The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following construction: multiplexer: “a device capable of manipulating multiple streams of digital information.”

The ordinary and customary meaning of “multiplexer” is a circuit that combines two or more input signals into a single output signal:

- **Multiplexer:** “a circuit combining two or more input signals into a single output signal for later recovery of the input signals.” (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 352-53.)
- **Multiplexer:** “a device that allows the transmission of two or more signals on a single line or in a single frequency channel.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 1426.)
- **Multiplexer:** “a device that allows two or more signals to be transmitted simultaneously on a single carrier wave, communications channel, or data channel.” (Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 433.)
- **Multiplexer:** “an electrical component which allows two or more coincident signals to be transmitted over a single channel.” (Ex. O, DICTIONARY OF ELECTRONIC PACKAGING, MICROELECTRONIC, & INTERCONNECTION TERMS at 91.)

The claim, however, further defines the claimed multiplexer—it must have an input coupled to the output of the register for receiving the parallel input data and must output serial data. The whole phrase should thus be construed for proper context. *See Phillips*, 415 F.3d at 1314.

Considering the entire phrase, the ordinary and customary meaning of “serial data” is data that is transmitted sequentially, one bit at a time:

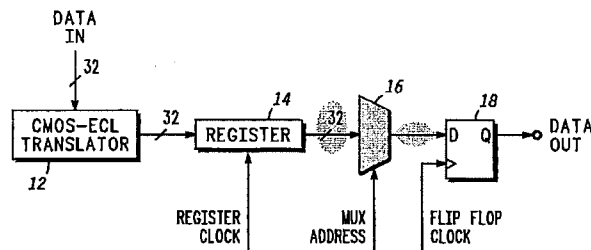
- **Serial data:** “data that is transmitted sequentially, one bit at a time.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 1960.)
- **Serial transfer:** “transfer of the characters of an element of information in sequence over a single path in a digital circuit.” (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 478.)
- **Serial:** “pertaining to the internal handling of data in sequential fashion.” (Ex. R, MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS at 1797.)

“Serial data” is thus separate and distinct from “parallel data”:

- **Serial:** “of or relating to the sequential handling of data items or instructions, *as opposed to parallel handling*.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 1960.)

- **Parallel:** “pertaining to the type of operation in a computer when all elements in an information item (bits in a word, e.g.,) are acted upon simultaneously *rather than serially (one at a time)*.” (Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 480.)

Consistent with the ordinary and customary meaning of the terms, the patent expressly differentiates “serial data” from “parallel data.” Indeed, the patent is directed to timing circuitry for performing “a parallel-serial conversion” or a “serial-parallel conversion.” (Ex. E at Abstract.) Asserted claim 8 is directed to “parallel-serial conversion”—it requires a register “for receiving parallel input data” and a multiplexer “for providing serial data” from the parallel input data. (Ex. E at 7:66-8:2.) For example, as illustrated by Fig. 1 (excerpted below), “[m]ultiplexer 16 rotates through the individual bit locations of register 14 under control of the MUX ADDRESS signal and provides serial bits to the data input of flipflop 18.” (Ex. E at 2:15-18.)



As explained by the specification, the multiplexer thus converts a “multi-bit signal” (*i.e.*, 32-bit parallel data) to “a string of data bits that are serially transmitted one at a time” (*i.e.*, serial data):

Parallel-serial converters are commonly used in digital circuit design to *convert multi-bit signals to a string of data bits that are serially transmitted one at a time.*

(Ex. E at 1:11-13.) Accordingly, consistent with the ordinary and customary meaning and the intrinsic record, the phrase should be construed as set forth by Samsung above.

3. “coupled”

Samsung's Construction	Defendants' Construction
The meaning of this term requires no construction. To the extent a construction is necessary, the term should be construed as “directly connected.”	“Linked together.”

Because the term “coupled” is not ambiguous or unclear, there is no need to construe this term. *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (“Claim construction ... is not an obligatory exercise in redundancy.”). Defendants, however, propose a construction not supported by the intrinsic record.

For example, claim 8 uses the term “coupled” to refer to two things: (i) the input of parallel data to the register; and (ii) the connection between the multiplexer and register:

- “a register having an input *coupled* for receiving parallel input data...” (Ex. E at 7:66-67.)
- “a multiplexer having an input *coupled* to said output of said register...” (Ex. E at 8:1-2.)

As described in the specification, those couplings are direct connections. Specifically, as shown in Fig. 1, register 14 directly receives 32-bit input data from logic translator 12. (Ex. E at 2:12-15.) Similarly, multiplexer 16 is directly connected to register 14. (Ex. E at 2:15-18.)

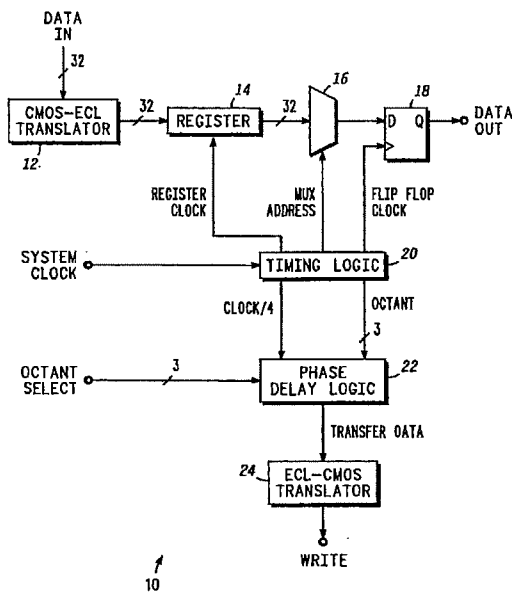


FIG. 1

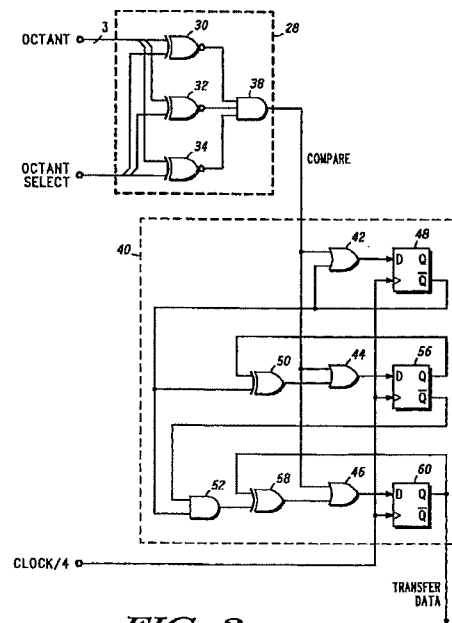


FIG. 2

Notably, the specification refers to a direct connection in every instance it uses the term “coupled” including, for example, the direct connections illustrated in Fig. 2 above:

The output of OR gate 42 is *coupled* to the D-input of flipflop 48. The Q-output of flipflop 48 is *coupled* to the second input of OR gate 42, to an input of exclusive-OR (XOR) gate 50, and to an input of AND gate 52. The output of XOR gate 50 is *coupled* to a second input of OR gate 44 that in turn has an output *coupled* to the D-input of flipflop 56. The Q-output of flipflop 56 is *coupled* to the second input of XOR gate 50, while the Q-output of flipflop 56 is *coupled* to the second input of AND gate 52. The output of AND gate 52 is *coupled* to a first input of XOR gate 58 that in turn has an output *coupled* to the second input of OR gate 46. The output of OR gate 46 is *coupled* to the D-input of flipflop 60. The Q-output of flipflop 60 is *coupled* to the second input of XOR gate 58 and further provides the TRANSFER DATA signal to ECL-CMOS translator 24 in FIG. 1.

(Ex. E at 3:49-64.) Accordingly, as used in the claims and specification, the term “coupled” means “directly connected.” See *PCTEL, Inc. v. Agere Sys., Inc.*, No. C03-02474 MJJ, 2006 WL 734385 at *6 (N.D. Cal. Mar. 20, 2006) (finding that the term “coupled” required a “direct connection” where “the inventor used ‘coupled’ and ‘connected to’ interchangeably and understood it as such.”); *Boston Scientific SciMed, Inc. v. EV3 Inc.*, 502 F. Supp. 2d 931, 937 (D. Minn. 2007) (construing “coupled” as “adjacent and directly connected to”).

4. “comparator”

Samsung's Construction	Defendants' Construction
A device whose output signal depends on the result of comparing two data items.	An electronic device that receives input from two or more sources and provides an output responsive to a comparison of the inputs.

The ordinary and customary meaning of a “comparator” is a device that provides an output signal that depends upon the result of comparing two data inputs:

- **Comparator:** “In a computer system, a device whose output signal depends on the result of its comparing two data items.” (Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 127.)
- **Comparator:** “a combinational electronic circuit that compares two numbers and determines their relative magnitude.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 479.)
- **Comparator:** “A device that compares two transcriptions of the same information to verify the accuracy of transcription, storage, arithmetical operation, or some other

process in a computer, and delivers an output signal of some form to indicate whether the two sources are equal or in agreement.” (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 105.)

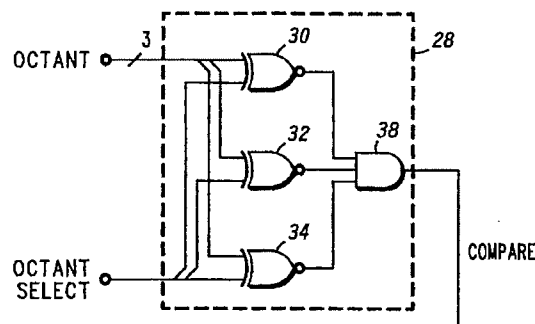
The claims and specification use the term in the same way. For example, claim 8 requires that the comparator provide an output that depends upon whether or not two input control signals match:

[A] comparator having *first and second inputs* and an output, said first input receiving a first control signal, said second input receiving said second control signal, said *output providing a compare signal having a first state when said first and second control signals match...*

(Ex. E at 8:3-7; *see also id.* at claims 5, 6, 12, 13.) Similarly, the specification provides that comparator 28 illustrated in Fig. 2 (excerpted below) receives two 3-bit input data signals—the “Octant” and “Octant Select” signals:

[D]igital comparator 28 ... receives bit0 of the OCTANT signal and bit0 of the OCTANT SELECT signal, ... bit1 of the OCTANT signal and bit1 of the OCTANT SELECT signal, [and] bit2 of the OCTANT signal and bit2 of the OCTANT SELECT signal.

(Ex. E at 3:31-38.)



And consistent with the ordinary and customary meaning, the specification explains that the output of comparator 28 depends upon the equivalency of the two 3-bit input data signals:

When the 3-bit OCTANT signal matches the externally-supplied 3-bit OCTANT SELECT signal, the COMPARE signal is asserted as logic one.

(Ex. E at 4:1-4; *see also id.* at 3:39-43, 4:27-42.) Accordingly, the term “comparator” should be construed as “a device whose output signal depends on the result of comparing two data items.”

5. “control signal”

Samsung's Construction	Defendants' Construction
A signal for controlling the phase of the transfer data signal.	A signal that conveys information about regulation or guidance.

Beginning with the words of the claim, it is clear that the sole function of the “control signals” is controlling the phase of the transfer data signal. For example, the control signals determine the state of the “compare signal,” which in turn causes the down counter to generate the appropriate transfer data signal:

[A] comparator having first and second inputs and an output, *said first input receiving a first control signal, said second input receiving a second control signal*, said output providing *a compare signal having a first state when said first and second control signals match*; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down *to generate a transfer data signal* having a symmetric duty cycle to enable transfer of said parallel input data to said register.

(Ex. E at 8:3-12.) The “control signals” thereby control the phase of a transfer data signal, and should be construed accordingly. *See Phillips*, 415 F.3d at 1314 (“To begin with, the context in which a term is used in the asserted claim can be highly instructive.”).

Consistent with the claim language, the specification explains that the patented invention is directed to timing circuitry for “controlling the phase of a data transfer signal” in parallel-serial or serial-parallel converters:

The present invention relates in general to digital timing circuits and, more particularly, *to controlling the phase of a data transfer signal* to set the proper timing for reading or writing to a data register.

(Ex. E at 1:7-10; *see also id.* at 6:13-15, Abstract, Title.) As illustrated by Fig. 1, the two signals input to phase delay logic 22 (which is illustrated in more detail in Fig. 2) that control the phase are the “Octant” and “Octant Select” signals:²

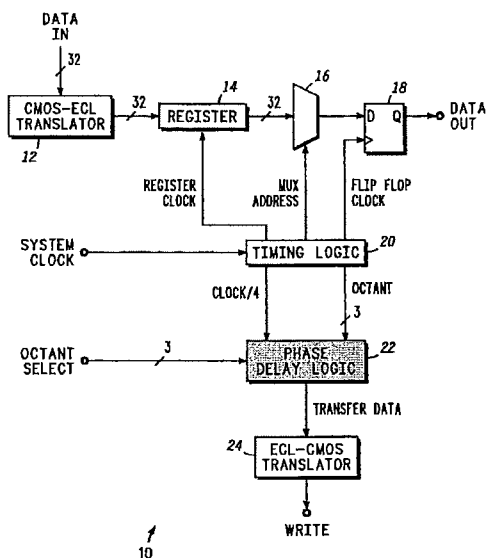


FIG. 1

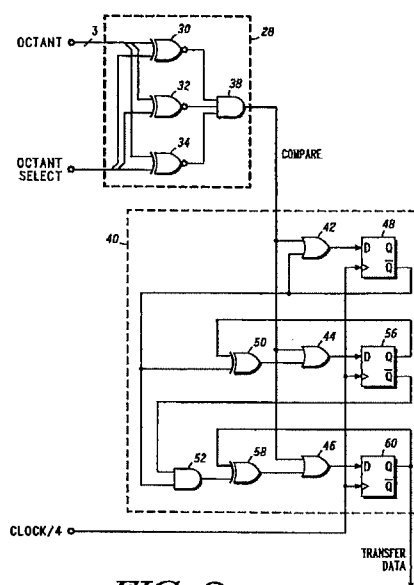


FIG. 2

(Ex. E at 2:62-64 (“Phase delay logic circuit 22 receives CLOCK/4 and OCTANT signals from timing logic 20, and an OCTANT SELECT signal from the external logic (not shown).”), 3:13-18, 3:40-42, 4:1-4, 6:1-3.) Indeed, there is no other function for the “Octant” and “Octant Select” control signals other than to control the phase. Accordingly, consistent with the claims and specification, the phrase “control signal” should be construed as set forth by Samsung above.

6. “first and second control signals match”

Samsung's Construction	Defendants' Construction
“The data represented by the first and second control signals is the same.”	The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions: control signals: (separately construed); match: “corresponding, suitably associated, or harmonious”

² As its name implies, the “CLOCK/4” signal is a clock signal for synchronization of the circuitry, not a “control signal.” (*See, e.g.,* Ex. E at 3:66-5:30, Fig. 2.)

Clam 8 requires “a *comparator* having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output *providing a compare signal having a first state when said first and second control signals match.*” (Ex. E at 8:3-7.) As discussed above, the ordinary and customary meaning of a “comparator” is a device with an output that depends upon the result of comparing two data inputs. The specification makes clear that such comparison is to determine whether or not the data represented by the first and second control signals are the same:

- “*When the 3-bit OCTANT signal matches the externally-supplied 3-bit OCTANT SELECT signal, the COMPARE signal is asserted as logic one.*” (Ex. E at 4:1-4.)
- “At the first rising edge of CLOCK/4 (clock C0), *the OCTANT signal is ‘000’ and does not match the OCTANT SELECT signal ‘001’.* Consequently, the COMPARE signal is logic zero.” (Ex. E at 4:27-31.)
- “At the second rising edge of CLOCK/4 (clock C4), *the OCTANT signal switches to ‘001’ and matches the OCTANT SELECT signal* causing the COMPARE signal goes to logic one.” (Ex. E at 4:32-35.)
- “*The OCTANT signal switches to ‘010’ and no longer matches the OCTANT SELECT signal.* The COMPARE signal returns to logic zero.” (Ex. E at 4:40-42.)

Accordingly, consistent with the claims and specification, the phrase should be construed as “the data represented by the first and second control signals is the same.”

7. “clock signal”

Samsung’s Construction	Defendants’ Construction
“A signal consisting of a series of pulses used for synchronizing the data conversion circuit.”	“A signal that conveys clocking or timing information.”

The ordinary and customary meaning of the phrase “clock signal” is “a signal consisting of a series of pulses used for synchronizing the data conversion circuit”:

- **Clock:** “A source of *accurately timed pulses for synchronization* in a digital computer or as a time base in a transmission system.” (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 92.)

- **Clock:** “A source of *accurately timed pulses, used for synchronization* in a digital computer or as a time base in a transmission system.” (Ex. R, MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS at 387.)
- **Clock:** “In a digital computer or control system, the device or circuit which supplies the *timing pulses that pace the operation of the digital system.*” (Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 115.)
- **Clock:** “1. a generator *used to synchronize the timing* in switching circuits and the speed of the central processing unit in a computer. 2. a device that *controls timing in a system, generally by generating a steady stream of pulses* at a tightly controlled constant rate.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 447.)
- **Clock pulses:** “A *train of signals* in which the separation between pulses is constant and *which serves to synchronize information transfer* among computer components.” (*Id.*)

The specification uses the phrase in the same way. For example, the specification describes several different clock signals, all derived from the main system clock:

Timing logic 20 operates in response to a SYSTEM CLOCK signal, running for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal is derived from dividing the SYSTEM CLOCK by value thirty-two....

Timing logic 20 further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four with alignment on the rising edges of SYSTEM CLOCK.

(Ex. E at 2:21-38.) Consistent with the ordinary and customary meaning, the specification explains that those clock signals function to synchronize various aspects of the data conversion circuit. (See, e.g., Ex. E at 1:14-19, 2:31-34, 3:66-4:1, 4:8-10, 4:24-5:23.) Accordingly, “clock signal” should be construed as set forth by Samsung above.

8. “transfer data signal”

Samsung's Construction	Defendants' Construction
“A periodic signal requesting that external logic write the next set of parallel input data to the register.”	“A signal that conveys information regarding the transfer of data.”

The '594 patent explains that the invention is directed to timing circuitry for controlling the phase of a data transfer signal to set the proper timing for reading or writing to the register:

The present invention relates in general to digital timing circuits and, more particularly, to controlling the phase of a data transfer signal to set the proper timing for reading or writing to a data register.

(Ex. E at 1:7-10; *see also id.* at 6:13-15, Abstract, Title.) As used in claim 8, the “transfer data signal” controls *writing* the next set of data to the register (as opposed to reading from the register). In that regard, claim 8 requires that the “transfer data signal” must have “a symmetric duty cycle *to enable transfer of said parallel input data to said register.*” (Ex. E at 8:10-12.)

Moreover, the stated goal of the patent is to provide maximum operating speed for data conversion by ensuring that each next set of data is requested at the appropriate time:

By now it should be appreciated that the present invention provides proper timing of the data transfer between external data sourcing or sinking logic and data conversion circuits.... Once the proper delay is determined by experimentation, the phase delay logic circuit asserts the transfer data signal at the correct time by controlling its phase, to allow maximum operating speed for the data conversion given the required set-up and hold-time of the embedded register and of the external logic. By controlling the phase of transfer data requests, the correct timing is established to ensure proper data set-up and hold times and to allow complete processing before the next data word needs to be read or written.

(Ex. E at 6:13-28; *see also id.* at 1:7-10, 1:57-59.) The specification thus explains that the “transfer data signal” is a periodic signal that requests more information at the proper time:

- *“The timing generation logic asserts a periodic signal to the external logic requesting data be presented to or removed from the data register.”* (Ex. E at 1:20-22.)
- *“When the periodic signal is asserted to the external logic, requesting that new data be read or written, the external logic begins the time-consuming process of retrieving or storing new data.”* (Ex. E at 1:33-36.)
- *“Accordingly, as a feature of the present invention, phase delay logic circuit 22 sets the timing of TRANSFER DATA signal by altering its phase as programmed by the 3-bit OCTANT SELECT signal to request more data at the proper time to allow*

parallel-serial converter 10 to complete processing the previous data." (Ex. E at 3:13-18.)

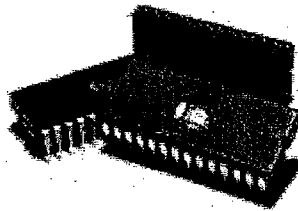
The "transfer data signal" described by the specification serves no other purpose. (*See, e.g.*, Ex. E at 3:13-18, 3:24-30, 4:17-23, 5:27-30.) The phrase should thus be construed in accordance with its use in asserted claim 8 and the specification as set forth by Samsung above.

IV. U.S. PATENT NO. 6,362,644

Defendants' '644 patent is directed to a technique for providing programmable termination for integrated circuits. (Ex. G at Title, Abstract, 1:39-46.) Claims 6-10, 12, and 16 are asserted in this case.

A. Background Of The '644 Patent Technology

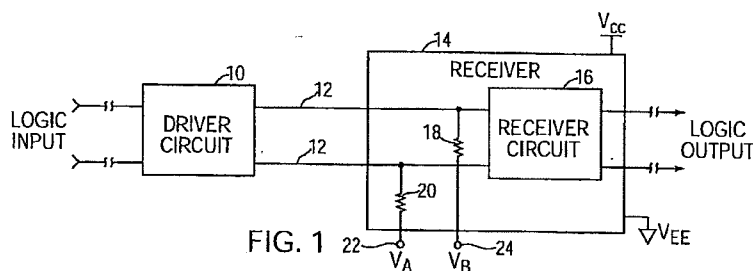
As illustrated below, integrated circuits may be enclosed in packages with external pins. (*See, e.g.*, Ex. G at 1:6-7, Title.)



Such circuits may be configured to communicate with each other by connecting their pins with a transmission line so that a signal can travel from one circuit (e.g., a "driver" circuit) to the other (e.g., a "receiver" circuit). (Ex. G at 1:17-21, 2:4-11.) A transmission line, however, has a physical property known as a "characteristic impedance," that results in a portion of a transmitted signal reflecting back from the receiver circuit if the receiver circuit does not exhibit the same impedance. (Ex. T, HOROWITZ & HILL at 879-881.) To avoid distortions caused by such signal reflection, a resistor matching the characteristic impedance of the transmission line may be provided at the end of the transmission line to "terminate" the line. (*Id.*; Ex. G at 1:21-29.)

Further complicating communications, integrated circuits may belong to different logic families such as ECL, CML, LVDS, CMOS, and TTL that represent signals differently. (Ex. G at 2:48-50; Ex. T, HOROWITZ & HILL at 565-575.) For example, a TTL circuit uses 3.5 volts to represent a “high” or “1” signal while a CMOS circuit uses its power supply voltage value to represent the same signal. (*Id.* at 572-575.) Accordingly, integrated circuits from two logic families may be unable to interoperate without accounting for their differences, such as by using a “translator” circuit. (*Id.*; Ex. G at 1:8-17.) Additionally, the transmission line may require a different “termination” depending upon the selected logic family. (Ex. G at 1:17-35.)

To facilitate interoperability between logic families, the '644 patent describes a technique whereby a circuit can be programmably terminated using external configuration pins. (Ex. G at Abstract, 1:39-46.) For example, Fig. 1 illustrates a receiver circuit 16 housed in a semiconductor package 14 having external configuration pins 22 and 24. (Ex. G at 2:6-7, 20-23.) The configuration pins 22 and 24 are connected to resistor load elements 20 and 18, respectively, and each of the load elements is connected to one of the transmission lines 12 to terminate the line. (Ex. G at 2:15-20.)



To programmably terminate a transmission line so that a circuit (e.g., receiver circuit 16) can communicate with another circuit (e.g., driver circuit 10) from a selected logic family, appropriate termination (*i.e.*, configuration) signals are applied to the configuration pins 22 and 24. (Ex. G at Abstract, 2:20-44.) For example, as shown in Fig. 1, if the driver circuit is from the ECL logic family, the configuration pins 22 and 24 are provided with a termination signal of

V_{CC}-2 volts to program the receiver circuit 16 to operate with an ECL driver circuit. (Ex. G at Abstract, 2:35-38, 4:46-56.) To program receiver circuit 16 to operate with a driver circuit from the CML logic family, the configuration pins 22 and 24 are provided with a termination signal of V_{CC}. (Ex. G at Abstract, 2:38-41, 4:46-56.) Accordingly, by applying different termination signals to configuration pins 22 and 24, receiver circuit 16 can be programmed to operate with driver circuits from various logic families. (Ex. G at Abstract, 2:20-44, 4:46-56.)

B. Proper Construction Of The Disputed Terms Of The '644 Patent

1. "termination signal" (claim 6) and "programmable termination" (claim 12)

Claim Term	Samsung's Construction	Defendants' Construction
"termination signal"	"A signal that configures the circuit to receive data signals from one of several available logic families."	"A signal that dissipates or absorbs energy."
"programmable termination"	"The capability to configure the circuit to receive data signals from one of several available logic families."	"An electrical circuit that can be configured to provide various levels or degrees for the dissipation or absorption of electrical energy."

The phrases "termination signal" in claim 6 and "programmable termination" in claim 12 do not have ordinary and customary meanings in the art. The proper construction of the phrases, however, are readily apparent from the intrinsic record. *See Phillips*, 415 F.3d at 1316 ("Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim.") (citation omitted). For example, as evidenced by the abstract, the entire focus of the '644 patent is providing programmability so that a receiver circuit can communicate with driver circuits from different available logic families:

A receiver circuit (16) is *programmable to operate with different logic family driver circuits* (10). The receiver circuit has two external configuration pins (22,) 24) that are *configured to provide the necessary termination for the type of logic family driver circuit used*.

(Ex. G at Abstract.)

Similarly, the specification repeatedly describes the programmability as the ability to configure the receiver circuit to communicate with different logic family drivers:

- ***“Configuration pins 22, 24 are external pins connected to receiver package 14 and are programmable so receiver circuit 16 can communicate with different logic family drivers. To program configuration pins 22, 24, the pins are terminated using a configuration which is dependent on the desired logic family application.”*** (Ex. G at 2:20-25.)
- ***“Configuration pins 42, 44 are external pins connected to receiver package 32 and are programmable so receiver circuit 34 can communicate with different logic family drivers. Configuration pins 42, 44 are programmed by terminating the pins using a configuration which is dependent on the desired logic family application.”*** (Ex. G at 3:2-7.)
- ***“Configuration pin 60 is an external pin connected to receiver package 52 that is programmable so receiver circuit 54 can communicate with different logic family drivers. Configuration pin 60 is programmed by terminating the pin using a configuration which is dependent on the desired logic family application.”*** (Ex. G at 3:51-56.)
- ***“A receiver circuit is programmable to configure different termination connections which allow the receiver circuit to communicate with a driver circuit from a different logic family.”*** (Ex. G at 4:58-62.)
- ***“A switch can be used to programmably connect termination pins 22, 24 to $V_{CC}-2$ for an ECL logic family application, or to V_{CC} for a CML logic family application. The switch can provide programmability for the termination signals to any of the previous configurations outlined herein.”*** (Ex. G at 4:52-56.)

As used in the patent, therefore, “programmable termination” refers to “the capability to configure the circuit to receive data signals from one of several available logic families.”

Similarly, the configuration of the circuit to receive data signals from one of several available logic families is determined by the “termination signals.” For example, as shown in Figs. 1 and 5, the “termination signals” are voltages (e.g., V_A and V_B) applied to the configuration pins (labeled 22 and 24 in Fig. 1, and 97 and 99 in Fig. 5) that configure the circuit to receive data signals from one of several available logic families.

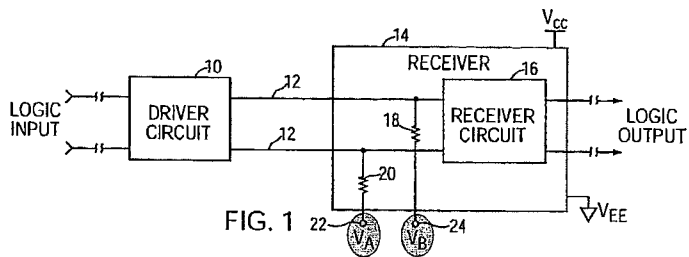


FIG. 1

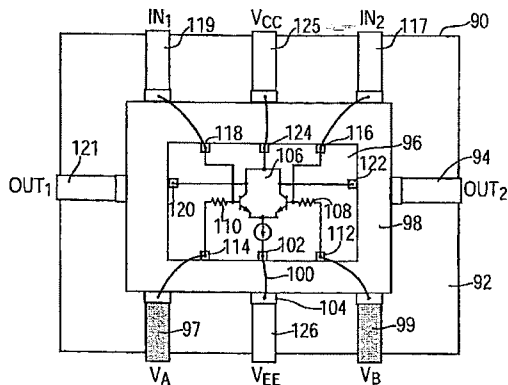


FIG. 5

(Ex. G at 2:25-43, 4:19-23, 4:32-35, 4:49-52; *see also id.* at Figs. 2-3, 3:8-34, 3:56-4:3.) Indeed, the specification expressly states that a “termination signal” is a **configuration** signal:

An alternative method to provide termination to any of the above embodiments is to use a switch between the termination (load) elements and the (**configuration**) **termination signals**.

(Ex. G at 4:46-49.) The term should therefore be construed in the same manner. *See Abbott Labs. v. Andrx Pharms., Inc.*, 452 F.3d 1331, 1344-45 (Fed. Cir. 2006) (upholding district court finding that “taste profile” has the same meaning as “taste perversion” because the patent “describes ‘taste profile’ in parentheses immediately following the words ‘taste perversion.’”); *Tate Access Floors, Inc. v. Maxcess Techs., Inc.*, 222 F.3d 958, 968 (Fed. Cir. 2000) (finding “inner layer” should be construed in the same manner as “inner body portion” because they are used interchangeably in the specification). Accordingly, a “termination signal” is “a signal that configures the circuit to receive data signals from one of several available logic families.”

2. “third and fourth pins for respectively receiving first and second termination signals” (claim 6) and “first and second load elements are coupled to third and fourth pins of the semiconductor package to provide a programmable termination” (claim 12)

Claim Term	Samsung's Construction	Defendants' Construction
“third and fourth pins for respectively receiving first and second termination signals”	“Third and fourth pins that receive different termination signals (e.g., not power supply or ground pins) dependant upon the selected one of several available logic families.”	The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions: “pins”; and “termination signals.”
“first and second load elements are coupled to third and fourth pins of the semiconductor package to provide a programmable termination”	“The first and second load elements are connected to the third and fourth pins that receive different signals to configure the circuit to receive data signals from one of several available logic families.”	The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions: “load elements”; “coupled”; “pins”; “semiconductor package”; “programmable termination.”

It is clear from the claims themselves that the third and fourth pins are configuration pins, and thus cannot be power supply or ground pins. For example, claim 6 requires that those pins receive “first and second termination signals,” and claim 12 requires that those pins “provide a programmable termination.” As discussed above, “termination signals” and “programmable termination” provide the capability of configuring the circuit to receive data signals from one of several available logic families. Such programmability cannot be accomplished with predefined power supply or ground potentials. Rather, there must be separate configuration pins, thereby allowing application of different termination signals based upon the selected configuration. Moreover, the claims themselves differentiate between the “third and fourth pins” and the power supply pins—claim 6 requires a “supply pin coupled for receiving a power supply voltage” and dependent claim 16 requires “applying a power supply voltage to a fifth pin.”

The specification also makes clear that the claimed third and fourth pins are *configuration pins* for configuring the circuit to receive data signals from one of several available logic families, rather than power supply pins. For example, as illustrated in Figs. 1 and 5, “ V_{CC} and V_{EE} are power supply potentials to receiver package 14 providing power to receiver circuit 16.” (Ex. G at 2:7-9.)

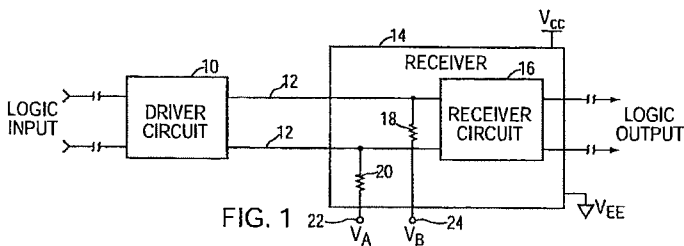


FIG. 1

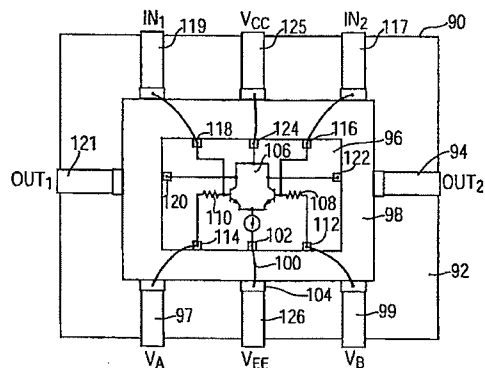


FIG. 5

The claimed third and fourth pins, to the contrary, are separate configuration pins for receiving configuration signals V_A and V_B . Indeed, the specification repeatedly and consistently refers to those pins as “configuration pins.” (Ex. G at Abstract, 2:16-43 (referring to “configuration pin 22” and “configuration pin 24” of Fig. 1), 2:65-3:34 (referring to “configuration pin 42” and “configuration pin 44” of Fig. 2), 3:47-4:5 (referring to “configuration pin 60” of Fig. 3), 4:12-14 (referring to “configuration pin 78” and “configuration pin 80” of Fig. 4), 4:19-23 (referring to “configuration pins 97, 99” of Fig. 5), 4:49-52 (referring to “external (configuration) termination pins 22, 24” of Fig. 1), 4:62-64.)

Moreover, during prosecution the inventors disclaimed from the scope of the claims circuitry wherein the load elements are connected to a predefined power supply or ground potential rather than separate configuration pins, because unlike the claimed invention, such circuitry is capable of terminating signals from only a single logic family. During prosecution, the Patent Office Examiner rejected various pending claims under 35 U.S.C. § 102(b) as being

anticipated by one or more of the following prior art references: (i) U.S. Patent No. 5,731,711 to Gabara; (ii) U.S. Patent No. 5,374,861 to Kubista; and (iii) U.S. Patent No. 5,781,028 to Decuir. (Ex. H at H-58-61.) To overcome the rejections, the inventors canceled a number of the pending claims, added new claims 27 and 33,³ among others, and explained to the Patent Office and the public how the new claims differed from the cited prior art. (Ex. H at H-71-79.)

Notably, the inventors distinguished both asserted independent claims from each of the three cited prior art references because those references disclosed coupling the load elements to a power supply or ground potential rather than to separate third and fourth configuration pins that received termination signals. The inventors additionally told the Patent Office and the public that because the prior art did not disclose coupling the load elements to separate third and fourth pins of the semiconductor package for receiving termination signals (e.g., configuration signals), the prior art could not terminate signals from a variety of logic families as required by the patent:

Inventors' Arguments To Obtain Claim 6:

- “The Gabara controllable impedance element is *coupled from interface 103 to internal nodes providing a power supply voltage V_R , V_P or V_{SS} , not to a third or fourth pin to receive a first or second termination signal*. Consequently, *the Gabara integrated circuit is suitable for terminating signals from a specified logic family, whereas the invention as claimed can terminate signals of a variety of logic families* because its load elements are coupled to third and fourth pins of a semiconductor package in order to receive first and second termination signals.” (Ex. H at H-75.)
- “The Kubista termination resistors are *coupled from lines 16 or 18 to either power supply V_{CC} or ground potential, not to third or fourth pins to receive first or second termination signals*. Consequently, *the Kubista termination network is suitable for terminating differential signals but does not have the flexibility of the claimed invention in terminating signals from a variety of logic families*, depending on the value of the first and second termination signals.” (Ex. H at H-76.)

³ Claims 27 and 33 were later renumbered and issued as asserted claims 6 and 12.

- “The Decuir termination resistor is *coupled either across the transmission line or to an existing power supply node such as V_{CC} or ground potential, not to a third or fourth pin that receives a termination signal*. Since the Decuir termination network does not have a load element coupled to a termination signal, *the termination network cannot be used to terminate signals from a different logic family by modifying a termination signal, as can the present invention.*” (Ex. H at H-76.)

Inventors’ Arguments To Obtain Claim 12:

- “The Gabara controllable impedance element is *coupled from interface 103 to internal nodes providing a power supply voltage V_R , V_P or V_{SS} , not to a third or fourth pin to provide a programmable termination* for first and second logic signals. Consequently, *the Gabara integrated circuit can terminate signals from a single family, whereas coupling the load elements of the claimed invention to third and fourth pins allow the load elements to terminate signals of a variety of logic families.*” (Ex. H at H-77-78.)
- “The Kubista termination resistors are *coupled to either power supply V_{CC} or to ground potential, not to third or fourth pins of a semiconductor package to provide a programmable termination* for first and second logic signals. Consequently, *the Kubista termination network terminates differential signals, whereas the claimed method is applicable to logic signals of a variety of logic families* because the third and fourth pins provide a programmable termination.” (Ex. H at H-78.)
- “The Decuir transmission line is loaded with a termination resistor *coupled either across the transmission line or to an existing power supply node such as V_{CC} or ground potential*. Since the Decuir termination resistor is not coupled to a third or fourth pin of a semiconductor package, it does not provide a programmable termination of first and second logic signals. Hence, use of *the Decuir device is limited to a suitable logic family, whereas the claimed method provides a programmable termination and therefore can be used with a variety of logic families.*” (Ex. H at H-79.)

Having repeatedly argued that their claimed invention was different from the prior art because “*the invention as claimed can terminate signals of a variety of logic families*” (Ex. H at H-75), Defendants are not entitled to “a mulligan that would erase from the prosecution history the inventor’s disavowal” of claim scope. *Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 957 (Fed. Cir. 2000); *see also Computer Docking Station Corp. v. Dell, Inc.*, Nos. 2007-1169 and 2007-1316, ___ F.3d ___, 2008 WL 752675 at *4 (Fed. Cir. Mar. 21, 2008) (“A patentee could [disavow claim scope], for example, by clearly characterizing the

invention in a way to try to overcome rejections based on prior art.”); *Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004); *Alloc v. Int’l Trade Comm’n*, 342 F.3d 1361, 1372 (Fed. Cir. 2003). The claims cannot, therefore, properly be construed to cover circuitry capable of terminating signals from only a single logic family. *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304 (Fed. Cir. 1997) (“[S]ince, by distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover, he is by implication surrendering such protection.”). Accordingly, the third and fourth pins must receive termination signals (e.g., they are not power supply or ground pins) that are dependent upon the selected one of several available logic families, as set forth by Samsung’s construction above.

3. “pin”

Samsung’s Construction	Defendants’ Construction
“A small diameter metal rod used as an electrical terminal external to the semiconductor package housing.”	“A conductor configured to make an electrical connection.”

The term “pin” in asserted claims 6, 8-10, 12, and 16 of the ’644 patent should be construed in accordance with its ordinary and customary meaning in the art as “a small diameter metal rod used as an electrical terminal external to the semiconductor package housing”:

- **Pin:** “A small diameter metal rod used as an electrical terminal and/or a mechanical support. They are used inside a package to support a wire bond and externally as a plug-in type connection. They are either straight or modified as a nail-head, upset-pierced, or a formed variety.” (Ex. O, DICTIONARY OF ELECTRONIC PACKAGING, MICROELECTRONIC, & INTERCONNECTION TERMS at 101.)
- **Pin:** “A metal lead or terminal that projects from an active or passive component package. It plugs into a hole in a circuit board or a socket for the transmission of input/output (I/O) signals or to receive power.” (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 401.)
- **Pin:** “A slender, straight, stiff prong used as a terminal or locking device.” (Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 500.)

The intrinsic record consistently uses the term “pin” in accordance with its ordinary meaning. For example, the claims require that the pins are the part of the semiconductor package that receive external signals. (Ex. G at claim 6, 5:57-6:3 (“... a semiconductor package having first and second pins respectively adapted for receiving first and second data signals, third and fourth pins for respectively receiving first and second termination signals, and a supply pin coupled for receiving a power supply voltage”); *see also id.* at claim 12, 6:31-33, 6:36-38.) The pins must, therefore, be external to the semiconductor package housing.

Consistent with the claims, the specification repeatedly and consistently provides that the pins are external to the housing:

- “*The configuration pins are external to a semiconductor package* (14) housing the receiver circuit.” (Ex. G at Abstract.)
- “*Configuration pins 22, 24 are external pins* connected to receiver package 14....” (Ex. G at 2:20-21.)
- “*Configuration pins 42, 44 are external pins* connected to receiver package 32....” (Ex. G at 3:2-3.)
- “*Configuration pin 60 is an external pin* connected to receiver package 52....” (Ex. G at 3:51-52.)
- “*The configuration pin is external to a semiconductor package* housing the receiver circuit.” (Ex. G at 4:65-66.)

Indeed, the specification indicates that by providing *external* configuration pins, the key benefit of the invention—providing easy termination options—may be achieved. (Ex. G at 4:66-5:3 (“Having configuration pins external to the semiconductor package provides for easy portability among different logic families, and easy termination options which require no additional translators to operate a mixed logic family system.”).)

Similarly, figure 5 illustrates that each of the pins 94, 97, 99, 117, 119, 121, 125, and 126, are external to the semiconductor package 90:

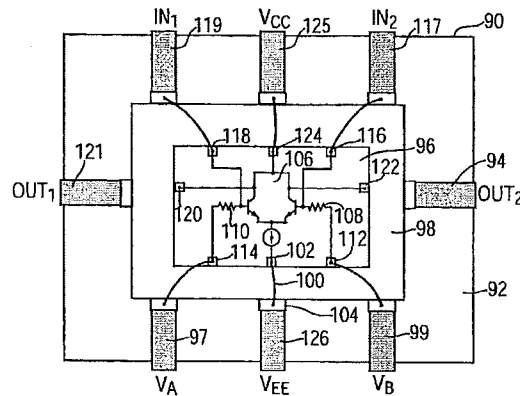


FIG. 5

(See also Ex. G at 4:17-19 (“Semiconductor package 90 houses a leadframe 92 with metal leads similar to lead 94 which provide input and output signals.”).) Notably, the specification differentiates those external pins from contacts that are not rod shaped such as the internal “bump type technology” or “ball grid array (BGA) technology” used to connect those pins to the bond pads 102, 112, 114, 116, 118, 120, 122, and 124. (Ex. G at 4:25-31.) Accordingly, the Court should construe the term “pin” in accordance with its ordinary and customary meaning and the intrinsic record as set forth by Samsung above.

4. “coupled”

Samsung’s Construction	Defendants’ Construction
The meaning of this term requires no construction. To the extent a construction is necessary, the term should be construed as “directly connected.”	“Linked together.”

As used in the claims, the term “coupled” is not ambiguous or unclear, so there should be no need to construe this term. *U.S. Surgical*, 103 F.3d at 1568. Defendants, however, propose a construction that is not supported by the intrinsic record. Contrary to Defendants’ proposal, the patent uses the term in two ways—to describe the physical relationship between circuit components and to describe application of signals to pins of the semiconductor package. Both uses of the term in the patent require a direct connection. Accordingly, to the extent the Court

construes the term “coupled” in asserted claims 6, 8-10, and 12, it should be construed in accordance with the intrinsic record as “directly connected.”

In several instances, the asserted claims use the term “coupled” to describe a direct electrical connection between semiconductor circuit components:

- “a first load element *coupled between the first and third pins* to terminate the first data signal...” (Ex. G at claim 6, 6:6-7.)
- “a second load element *coupled between the second and fourth pins* to terminate the second data signal...” (Ex. G at claim 6, 6:7-9.)
- “first and second load elements are *coupled to third and fourth pins* of the semiconductor package...” (Ex. G at claim 12, 6:36-38.)

The patent specification describes those elements as being *connected*. As shown in Fig. 1, “[l]oad element 18 is *connected* to configuration pin 24 and load element 20 is *connected* to configuration pin 22.” (Ex. G at 2:16-18; *see also id.* at 2:65-67, 3:47-49.) Similarly, as shown in figure 5, “[l]oad elements 108, 110 are *connected* to bond pads 112, 114 respectfully to *provide an electrical connection* to configuration signals V_B and V_A .” (Ex. G at 4:32-35.)

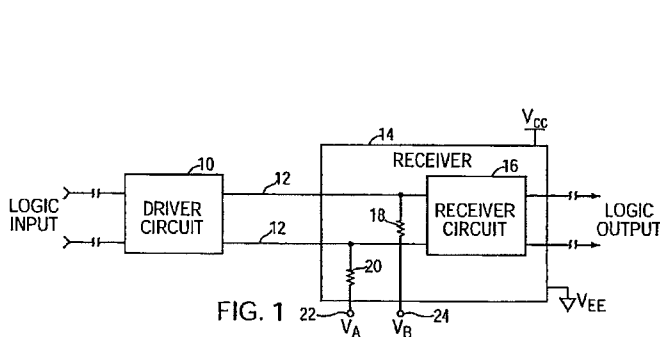


FIG. 1

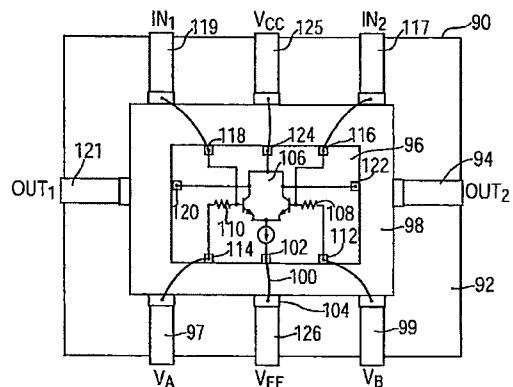


FIG. 5

As described by the intrinsic record, therefore, “coupled” refers to a direct electrical connection, e.g., a connection with no intervening circuit elements.

The claims also use the term “coupled” to describe signals that are directly applied to various pins of the semiconductor package:

- “first and second inputs *coupled* to the first and second pins, respectively...” (Ex. G at claim 8, 6:14-16.)
- “first and second outputs *coupled* to the first and second pins, respectively...” (Ex. G at claim 9, 6:18-20.)
- “the third pin is *coupled* for receiving a first termination voltage...” (Ex. G at claim 10, 6:22-23.)

The specification uses the term *connected* to refer to the same thing. (See, e.g., Ex. G at 2:35-38 (“For example, to terminate receiver circuit 16 for an ECL application requires configuration pin 22 (V_A) and configuration pin 24 (V_B) are *connected* to receive configuration signal, V_{CC} -2 volts.”), 3:23-34, 3:66-4:3.) Accordingly, as used in the claims and specification, the term “coupled” means “directly connected.” See, e.g., *PCTEL*, 2006 WL 734385 at *6; *Boston Scientific*, 502 F. Supp. 2d at 937.

5. “terminate” (claim 6) and “loading” (claim 12)

Claim Term	Samsung’s Construction	Defendants’ Construction
“terminate”	“The use of a load at the end of a transmission line or other device whose impedance is matched to that of the line.”	“To dissipate or absorb energy.”
“loading”	“Placing an impedance at the end of a transmission line or other device to match that of the line.”	“Applying effects that dissipate electrical energy.”

The ordinary and customary meaning of “terminate” in the art is the use of a load at the end of a transmission line or other device whose impedance is matched to that of the line:

- **Termination:** “The use of a load at the end of a transmission line or other device whose impedance, if matched to that of the line, will create no reflections.” (Ex. Q, ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY at 2189.)
- **Terminated line:** “A transmission line terminated in a resistance equal to the characteristic impedance of the line, so there are no reflections and no standing waves.” (Ex. P, MCGRAW-HILL ELECTRONICS DICTIONARY at 534.)
- **Termination:** “Load connected to a transmission line or other device; to avoid wave reflections, it must match the characteristic of the line or device.” (Ex. R, MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS at 2004.)

The claims and specification use the term in accordance with its ordinary and customary meaning. For example, claim 6 requires that “a first load element ... terminate the first data signal” and “a second load element ... terminate the second data signal” which are received from the transmission line on the first and second pins. (Ex. G at 6:6-9.) The specification likewise explains that the termination is a resistance typically chosen to equal the impedance of the transmission line:

The termination is a resistance that provides a termination for the logic device through to a voltage source V_{tt}. The voltage source V_{tt} is typically different for each logic family application. The resistance is typically chosen to equal the impedance of the interconnect transmission line to help reduce interconnect signal distortion.

(Ex. G at 1:20-27.) The term “terminate” should therefore be construed in accordance with its ordinary and customary meaning and use in the claims and specification as “the use of a load at the end of a transmission line or other device whose impedance is matched to that of the line.”

Claim 12 uses the term “loading” in the same way claim 6 uses the term “terminate”—claim 12 requires “**loading** the first and second logic signals with first and second load elements ... to provide a programmable termination.” (Ex. G at 6:34-38.) That use in the claim is consistent with the ordinary and customary meaning of the term. (See, e.g., Ex. S, THE ILLUSTRATED DICTIONARY OF ELECTRONICS at 389 (loading: “The matching of source impedance to load impedance, usually by means of the introduction of an inductance or capacitance into the load itself.”).) Accordingly, the term “loading” should be construed in accordance with its ordinary and customary meaning and use in the claims as “placing an impedance at the end of a transmission line or other device to match that of the line.”

6. "load element"

Samsung's Construction	Defendants' Construction
"An impedance that provides a termination for a logic device transmission line to help reduce interconnect signal distortion."	"Electrical devices capable of dissipating electrical energy."

Beginning with the words of the claims themselves, the "load elements" must provide the termination for the transmission line. For example, claim 6 requires "a first load element ... to terminate the first data signal" and "a second load element ... to terminate the second signal." (Ex. G at 6:6-9.) Similarly, claim 12 requires "first and second load elements ... to provide a programmable termination." (Ex. G at 6:36-38.) The phrase should therefore be construed accordingly. *See Phillips*, 415 F.3d at 1314 ("To begin with, the context in which a term is used in the asserted claim can be highly instructive.")

Additionally, the specification expressly states that the claimed "load element" is a **termination** element:

An alternative method to provide termination to any of the above embodiments is to use a switch between the **termination (load) elements** and the (configuration) termination signals.

(Ex. G at 4:46-49.) It is clear, therefore, that the claimed "load elements" refer to termination elements, rather than a generic electrical device as proposed by Defendants. *See Abbott Labs.*, 452 F.3d at 1344-45 (upholding district court finding that "taste profile" has the same meaning as "taste perversion" because the patent "describes 'taste profile' in parentheses immediately following the words 'taste perversion.'"); *Tate Access*, 222 F.3d at 968 (finding "inner layer" should be construed in the same manner as "inner body portion" because they are used interchangeably in the specification).

Finally, the specification expressly provides that the termination (e.g., load) element is a resistance typically chosen to equal the impedance of the transmission line:

The termination is a resistance that provides a termination for the logic device through to a voltage source V_{tt}. The voltage source V_{tt} is typically different for each logic family application. *The resistance is typically chosen to equal the impedance of the interconnect transmission line to help reduce interconnect signal distortion.*

(Ex. G at 1:20-26.) Accordingly, the Court should construe the term “load element” in accordance with its use in the intrinsic record as set forth by Samsung above.

V. U.S. PATENT NO. 5,252,177

The '177 patent is the Samsung patent-in-suit. Samsung believes there are only two terms or phrases that should be construed. Defendants originally proposed fourteen terms to be construed, but have continued to reduce that number and change the proposed terms and phrases up to the present time. As a result, in some instances, the proposed terms and phrases do not match those in the Joint Submission—Samsung has attempted herein to incorporate Defendants' changes and respond appropriately.

Even with the changes, for the most part, the terms and phrases selected by Defendants for construction do not require construction. Claim construction is not “an obligatory exercise in redundancy.” *See U.S. Surgical*, 103 F.3d at 1568. As explained below, Defendants' proposed constructions do not seek to resolve disputed ordinary meanings of claim terms or resolve contextual issues as to claimed phrases, but rather seek to improperly read limitations and preferred embodiments into ordinary meanings of otherwise unambiguous phrases. Stripped of those read-in limitations, the terms and phrases require no construction. *See, e.g., Biotec Biologische Naturverpackungen GmbH v. Biocorp, Inc.*, 249 F.3d 1341, 1349 (Fed. Cir. 2001) (deciding that the disputed issue was the proper application of a claim term rather than the scope of the term). Nonetheless, Samsung has provided alternative constructions for those terms and phrases in the event the Court believes construction is necessary. Samsung has also attempted to group related terms and phrases for the convenience of the Court.

A. Background Of The '177 Patent Technology

The '177 patent is directed to a method for manufacturing semiconductor devices having multiple wiring levels. (Ex. I at 1:6-8.) Such multiple wiring level semiconductor devices or integrated circuits are commonplace today. But at the time of the '177 patent invention in 1991, there were many technical obstacles to manufacturing a device with more than one metal layer.

As described in the background of the '177 patent, the conventional method for manufacturing a semiconductor device with multiple wiring levels included: depositing a first insulating layer 5 over the semiconductor substrate; depositing a first conductive layer 7 over the insulating layer; depositing a second insulating layer 9 over the top of the first conductive layer 7; depositing a second conductive layer 11 over the second insulating layer 9; and then depositing a third insulating layer 13 over the top of the second conductive layer 11. (Ex. I at 1:24-31.) The result is two conductive layers sandwiched between insulating layers. (*See, e.g.*, Ex. I at Fig. 1A.) Additional conductive layers can be added in the same fashion. These horizontal metal layers act as wiring layers in the semiconductor, as shown in Fig. 1A.

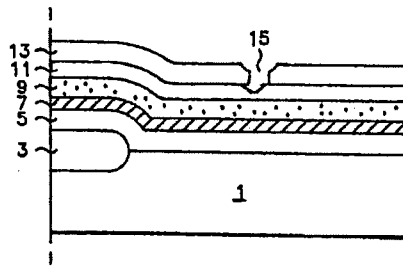


Fig. 1A
(Prior Art)

To connect two conductive layers together, a vertical contact hole 15 must be formed through the intermediate insulating layer to reach the underlying conductive layer. (Ex. I at 1:31-33.) The '177 patent describes how a contact hole can be formed through an etch process. (*Id.*) First, a layer of photoresist is placed over the insulating layer. Next, the light sensitive photoresist is patterned through photolithography. The pattern has openings where the holes are

to be etched and otherwise covers the layer. An etch, such as a plasma etch, is then applied to remove the insulating layer in the openings of the photoresist pattern. The insulating layer is not etched in those portions covered by the photoresist. After the hole is formed in the insulating layer to the underlying conductive layer, the photoresist is removed. (Ex. I at 1:50-57.) Photoresist is removed through the conventional process of plasma ashing, followed by cleaning. (*Id.*) Plasma ashing is an etch that includes use of a gas that reacts with the photoresist, and which results in the photoresist turning to carbon oxide gases. (*See* Ex. U at 1:5-8, 1:15-21, 1:26-34, 2:20-34.) The substrate is cleaned of any remaining photoresist or residuals, for example, by using organic solvents, rinsing with water, and drying. (Ex. I at 1:50-57.) The contact hole can now be filled with metal to form a vertical conductive connection between the metal layers. (Ex. I at 1:65-67.)

The '177 patent describes a problem with this process. After forming the contact hole, the cleaning materials used after the plasma etching may chemically interact with the underlying conductive layer if it is made of metal. In particular, the '177 patent describes how aluminum with added copper is particularly susceptible to this problem: "the copper component existing in [sic] grain boundary of the aluminum is discolored with spots and pieces of the [] conductive layer 11 may drop away. The size of these pieces can be 1 μ m in diameter. The resultant damage to the wiring is shown in FIG. 1A." (Ex. I at 1:59-64.)

The '177 patent inventors solved this problem by creating a protective oxide layer over the metal wiring layer before removing the remaining photoresist. (Ex. I at 3:2-8.) The protective oxide layer can be formed during the plasma ashing removal step and the '177 patent describes exemplary ashing process parameters to form this oxide. (Ex. I at 2:61-3:2.) In this way, the photoresist can be removed in conventional fashion and the integrity of the underlying conductive layer can be preserved.

B. Proper Construction Of The Disputed Terms Of The '177 Patent**1. "photoresist pattern"**

Samsung's Construction	Defendants' Construction
The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as "a layer of photoresist material that selectively exposes an underlying layer."	"A light sensitive organic material formed into a predetermined pattern and that can be removed in oxygen plasma."

There is no need to construe this commonplace and well known term in the semiconductor manufacturing field. It refers to the layer of photoresist material that selectively exposes an underlying layer. (Ex. I at 1:31-33.) There is no need to further define photoresist, which is a well known term to those in the art, and defined in numerous technical dictionaries. (See, e.g., Ex. BB, MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS at 1420; Ex. V, MICROCHIP FABRICATION at 511; Ex. N, MODERN DICTIONARY OF ELECTRONICS at 743.) To the extent any definition of "photoresist" is necessary, these general definitions should be adopted.

Defendants seek to limit "photoresist" to the preferred embodiment described in the patent. In particular, Defendants seek to limit the "photoresist patterns" to (1) only those photoresists made of organic materials and (2) only those that can be removed through an oxygen plasma. While these characteristics are exemplary of many photoresists, it is not a necessary characteristic of all photoresists. Indeed, Defendants' own dictionary definition places no such restrictions on the general definition of photoresist. (See Ex. W, COMPREHENSIVE DICTIONARY OF ELECTRICAL ENGINEERING at 487 (photoresist: "a photosensitive material that forms a three-dimensional relief image by exposure to light and allows the transfer of the image into the underlying substrate (for example, by resisting an etch)").) Nor does any basis exist in the intrinsic evidence to unduly limit the type of photoresist claimed in the invention. Accordingly, Defendants' proposed construction attempting to read in embodiments should be

rejected. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 908-09 (Fed. Cir. 2004) (refusing to limit asserted claims to embodiments disclosed in the specification because the portions of the specification disclosing those embodiments “do not expressly or by clear implication restrict the scope of the invention”).

2. “expose a top surface of said first conductive layer”

Samsung's Construction	Defendants' Construction
The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “exposing a top surface of a layer of electrically conductive material.”	“The uppermost surface of the unoxidized conductive layer is uncovered by the etching step.”

This phrase requires no construction. It simply means exposing a top surface of a layer of electrically conductive material. (Ex. I at Fig. 1A, 1:31-35.) There are no terms that require construction and the overall phrase should be read in its ordinary meaning.

Defendants identify no disputed ordinary meaning for any term or any confusion over the language used in the phrase. Instead Defendants seek to improperly read multiple limitations into the otherwise straightforward phrase, including (1) how the top surface is exposed; (2) the material choice of the electrically conductive layer; and (3) the condition of the “top surface” of the conductive layer (*i.e.*, “unoxidized”). The intrinsic evidence provides no support for Defendants’ special meaning of the disputed phrase. To the extent these terms are subject to further limitations, those limitations are recited in the body of the claim. Accordingly, Defendants’ proposal should be rejected.

3. **“removing said photoresist pattern positioned on said insulation layer by plasma etching simultaneously forming a protective oxide layer”** (claim 1) and **“removing remaining photoresist positioned on said insulation layer by plasma ashing to simultaneously form a protective oxide layer on said exposed top surface of said first conductive layer”** (claim 8)

Claim Term	Samsung's Construction	Defendants' Construction
<u>“removing said photoresist pattern positioned on said insulation layer by plasma etching simultaneously forming a protective oxide layer”</u>	The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “removing photoresist on the insulating layer through plasma ashing / etching while also forming a protective oxide layer on the exposed top surface of the first conductive layer.”	“Getting rid of all the photoresist on the insulation layer by plasma etching and forming a protective oxide layer at the same time as removing the photoresist.”
<u>“removing remaining photoresist positioned on said insulation layer by plasma ashing to simultaneously form a protective oxide layer on said exposed top surface of said first conductive layer”</u>	The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “removing photoresist on the insulating layer through plasma ashing / etching while also forming a protective oxide layer on the exposed top surface of the first conductive layer.”	“Getting rid of all the remaining photoresist by plasma ashing and forming a protective oxide layer at the same time as removing the photoresist.”

Defendants changed their proposed phrase for construction on the eve of filing the Joint Statement from the underlined portion in the caption to the larger phrase identified above. (*Compare* Ex. X, Defendants' Preliminary Proposed Claim Constructions at 10 with Final Joint Claim Construction Charts Ex. F at 33, 36-37 (D.I. 90).) Although Samsung had no opportunity to respond then, the changed position in proposed construction leads to the same result. There is nothing in the new proposed phrase that requires any clarification or construction. It means removing photoresist on the insulating layer through plasma ashing / etching while also forming a protective oxide layer on the exposed top surface of the first conductive layer. This unambiguous meaning is explained in the specification at column 2, line 62 to column 3 line 2.

(Ex. I at Fig. 1A, 2:62-3:2.) The individual terms in the phrase, like “plasma ashing,” are not part of Defendants’ proposed construction.

Defendants’ proposed construction attempts to improperly read into this phrase limitations that are inconsistent with the specification. Defendants propose that this step gets rid of “all” of the photoresist through the plasma etch or ashing. To be sure, the plasma ashing removes the photoresist. (Ex. I at 1:50-57.) But the specification also recognizes that there may be a need to perform “subsequent processing to remove the photoresist” *after* the ashing step. (Ex. I at 3:2-7.) Indeed, Defendants’ own construction of “protective oxide layer” below recognizes this fact. *See* § V.B.6, *infra*. Neither the patent laws nor the ’177 patent specification require such scientific perfection that “all” or 100% of the remaining photoresist is removed. *See Conoco, Inc. v. Energy & Env’tl. Int’l, L.C.*, 460 F.3d 1349, 1360-61 (Fed. Cir. 2006) (holding that an accused mixture infringes, even though it contains minor impurities not expressly allowed by the claim, because one of skill in the art would understand the claimed mixture to include those minor impurities). As a result, Defendants’ proposed construction reads limitations into the claims, contrary to the specification. Defendants’ proposal should be rejected.

4. “plasma etching” and “plasma ashing”

Claim Term	Samsung’s Construction	Defendants’ Construction
“plasma etching”	The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “a process of removing one or more materials using plasma.”	This claim is invalid for failure to comply with the requirements of 35 U.S.C. § 112. To the extent the Court construes this term, ON Semiconductor contends that the phrase can be understood with the following construction: plasma etching: “An etching process for forming a contact hole using a plasma of ionized gases in which the ions are accelerated toward the material desired to be removed.”

“plasma ashing”	The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “a plasma etch designed to remove photoresist.”	This claim is invalid for failure to comply with the requirements of 35 U.S.C. § 112. To the extent the Court construes this term, ON Semiconductor contends that the phrase can be understood with the following construction: plasma ashing: “A process for removing an organic material, such as a photoresist in a plasma of oxygen.”
-----------------	---	---

“Plasma etching” and “plasma ashing” are two common terms in the semiconductor manufacturing field that Samsung submits require no construction other than rejecting Defendants’ attempts to read in limitations. A plasma etch is a “a process of removing one or more materials using plasma.” That is how the term is used in the patent. (Ex. I at 1:31-33.) That is how the term is used in the field. *See, e.g., Agere Sys., Inc. v. Atmel Corp.*, 2004 WL 945162 at *19 (E.D. Pa. Apr. 30, 2004) (defining “etch” and determining plasma etch is within its scope) (*see also* Ex. N, MODERN DICTIONARY OF ELECTRONICS at 754 (plasma etching: “An etching process using a cloud of ionized gas as the etchant.”)). Plasma ashing is a plasma etch designed to remove photoresist. That is how the term is used in the patent. (*See, e.g.,* Ex. I at 2:61-63.) That is how the term is used in the field. (*See, e.g.,* Ex. U at 1:5-8, 2:20-21.)

Defendants do not genuinely dispute the ordinary meaning of “plasma etch.” Instead, Defendants seek to limit the term “plasma etch” to only those plasma etches that are used to make contact holes. That construction is inconsistent with the term’s ordinary meaning as reflected by both parties’ extrinsic evidence. (*See, e.g.,* Ex. N, MODERN DICTIONARY OF ELECTRONICS at 754; Ex. Y, Burba et al., *Selective Dry Etching of Tungsten for VLSI Metallization*, 133 J. OF THE ELECTROCHEMICAL SOC’Y at 2113.) A plasma etch can etch any structure, not just contact holes. More importantly, Defendants’ construction is inconsistent with the ’177 patent specification that recognizes that a plasma etch may be used to remove photoresist. (Ex. I at claim 8, 4:34-37.)

Similarly, Defendants do not genuinely contest the ordinary meaning of plasma ashing as a plasma etch to remove photoresist. Rather, they seek to limit the meaning of plasma ashing to only those plasmas made of oxygen gas and only those designed to remove organic materials. While this is the preferred embodiment of the invention, there is no basis to read that preferred embodiment into the claims. Accordingly, Defendants' construction should be rejected.

5. “simultaneously form[ing] a protective oxide layer” and “simultaneously form[ing]”

Claim Term	Samsung's Construction	Defendants' Construction
“simultaneously form[ing] a protective oxide layer”	“During the process of removing photoresist through plasma ashing / etching, creating an oxide layer sufficient to protect the underlying first conductive layer.”	“Forming at the same time.”
“simultaneously form[ing]”	“Forming as part of the plasma ashing / etching also used to remove photoresist.”	“Form at the same time.”

Samsung groups together these two related phrases. One is a subpart of the other. Samsung contends that only the larger phrase needs to be construed. The related phrases appear in two different claims. The principal distinction between the use of the disputed phrases in the two claims is that in claim 1 the photoresist is removed by plasma etching and in claim 8 the photoresist is removed by a particular type of plasma etch, *i.e.*, plasma ashing. (*Compare* Ex. I at claim 1, 3:59-4:2 *with* claim 8, 4:34-37.) There is no reason to construe the meaning of “simultaneously form” in the abstract—the issue is what does “simultaneously form” mean in the context of its relationship with the protective oxide layer. The overall phrase means “during the process of removing photoresist through plasma ashing or etching, creating an oxide layer sufficient to protect the underlying first conductive layer.” If the constituent term “simultaneously form” of the overall phrase needs to be construed, it means “forming as part of the plasma ashing / etching also used to remove photoresist.”

Samsung's construction is consistent with the use of the phrase in the patent. At col. 2, line 61 to col. 3, line 2, the process parameters whereby the photoresist is removed and a protective oxide layer is generated are described. (Ex. I at 2:61-3:2.) Defendants' proposal ignores this relevant context. In proposing to construe the term "simultaneously form" in isolation, the proposed construction ignores what is formed at the same time as well as what "time" is being referred to, *i.e.*, the recited step of removing photoresist. Accordingly, Defendants' proposed construction is incomplete, and Samsung's should be accepted.

6. "protective oxide layer"

Samsung's Construction	Defendants' Construction
"An oxide layer sufficient to prevent damage to an underlying layer."	"An oxide layer of a predetermined thickness (e.g., a thickness of 30 to 80 Å for an aluminum conductor) that is used to prevent damage to an underlying layer by preventing reaction between the wiring, an organic solvent and water in subsequent processing steps."

The meaning of this term in the claims of the '177 patent is an oxide layer sufficient to prevent damage to an underlying layer. That is the meaning used in the specification of the '177 patent. (Ex. I at 3:2-8, 3:23-28.) That is the ordinary meaning of "protective." (*See* Ex. Z, WEBSTER'S THIRD NEW INTERNATIONAL DICTIONARY at 1823 (protective: "something that serves for protection...."); Ex. AA, WEBSTER'S NINTH NEW COLLEGIATE DICTIONARY at 946 (protect: "to cover or shield from exposure, injury, or destruction....").)

Defendants' proposed construction attempts to read limitations into the claim. A "protective" layer need not be "predetermined" nor must it be "30 to 80 Å for an aluminum conductor." It simply needs to prevent damage to the underlying layer. (Ex. I at 3:7-8 ("Because of the above result, the wiring is protected and not damaged.").) Defendants' proposed construction is improper in seeking to read limitations into the claims.

7. “exposed top surface”

Samsung's Construction	Defendants' Construction
The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “the exposed top surface of a layer of electrically conductive material.”	“The uppermost surface of the unoxidized conductive layer is uncovered by the etching step.”

This unambiguous term requires no construction. To the extent a construction is necessary, the phrase should be construed as “the exposed top surface of a layer of electrically conductive material.” (Ex. I at 1:31-35.)

Defendants’ proposed construction improperly reads into the term (1) the material choice of the object being modified by the term; and (2) how the surface is formed. Accordingly, Defendants’ improper attempt to read limitations into the claims should be rejected.

8. **“removing said oxide layer before forming a second conductive layer on said exposed top surface of said first conductive layer” (claim 1) and “removing said oxide layer before forming said second conductive layer on said exposed top surface of said first conductive layer” (claim 8)**

Claim Term	Samsung's Construction	Defendants' Construction
“removing said oxide layer before forming a second conductive layer on said exposed top surface of said first conductive layer”	The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “removing the protective oxide from the top surface of the first conductive layer before forming a second conductive layer.”	“Getting rid of the entire protective oxide layer before forming a second conductive layer such that the top surface of the first conductive layer is completely exposed”
“removing said oxide layer before forming said second conductive layer on said exposed top surface of said first conductive layer”	The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as “removing the protective oxide from the top surface of the first conductive layer before forming a second conductive layer.”	“Getting rid of the entire protective oxide layer before forming a second conductive layer such that the top surface of the first conductive layer is completely exposed.”

Defendants changed their proposed phrase for construction on the eve of filing the Joint Statement from the underlined portion in the caption to the larger phrase identified above.

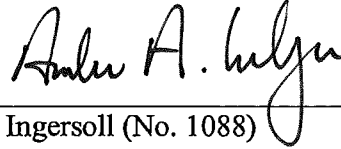
(Compare Ex. X, Defendants' Preliminary Proposed Claim Constructions at 11 with Final Joint Claim Construction Charts Ex. F at 36, 40-41 (D.I. 90).) Although Samsung had no opportunity to respond then, the changed position in proposed construction leads to the same result. There is nothing in the proposed phrase that requires any clarification or construction. It means removing the protective oxide from the top surface of the first conductive layer before forming a second conductive layer. The intrinsic evidence supports only this construction. (See, e.g., Ex. I at 3:8-13, claim 1, 4:3-5, claim 5, 4:16-17, claim 8, 4:38-40, claim 15, 4:57-59.)

Defendants now seek to construe this entire phrase in order to read in limitations. Defendants seek to read into the phrase that "all" of the photoresist be removed and that the "entire" top surface of the first conductive layer be exposed. While those requirements may satisfy the preferred embodiment, neither the '177 patent nor the patent laws require such 100% certainty. To the contrary, process variations, whether intentional or not, exist in the manufacture of any product. Nothing in the language of the claims or other intrinsic evidence provides any support for Defendants' attempts to require technical perfection, including that 100% of the oxide layer is removed and that the exposed top surface is completely exposed. And the patent laws recognize such perfection should not be read into claim constructions. See *Conoco*, 460 F.3d at 1360-61 (holding that the accused mixture infringes, even though it contains minor impurities not expressly allowed by the claim, because one of skill in the art would understand the claimed mixture to include those minor impurities). Accordingly, Defendants' proposed construction is improper and should be rejected.

CONCLUSION

For the foregoing reasons, Plaintiff Samsung respectfully requests that this Court construe, as a matter of law, the disputed terms of the patents-in-suit as set forth above.

YOUNG CONAWAY STARGATT &
TAYLOR, LLP



Josy W. Ingersoll (No. 1088)
John W. Shaw (No. 3362)
Andrew A. Lundgren (No. 4429)
The Brandywine Building
1000 West Street, 17th Floor
Wilmington, Delaware 19899-0391
302-571-6600
alundgren@ycst.com

*Attorneys for SAMSUNG ELECTRONICS CO.,
LTD., SAMSUNG ELECTRONICS AMERICA,
INC., SAMSUNG TELECOMMUNICATIONS
AMERICA GENERAL, L.L.C., SAMSUNG
SEMICONDUCTOR, INC., and SAMSUNG
AUSTIN SEMICONDUCTOR, L.L.C.*

OF COUNSEL:

John M. Desmarais
Jon T. Hohenthanner
James E. Marina
KIRKLAND & ELLIS LLP
153 East 53rd Street
New York, NY 10022-4611
212-446-4800
jdesmarais@kirkland.com
jhohenthanner@kirkland.com
jmarina@kirkland.com

Edward C. Donovan
KIRKLAND & ELLIS LLP
655 Fifteenth Street, N.W.
Washington, D.C. 20005-5793
202-879-5000
edonovan@kirkland.com

Dated: April 14, 2008

CERTIFICATE OF SERVICE

I, Andrew A. Lundgren, Esquire, hereby certify that on April 14, 2008, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to the following counsel of record:

Karen Jacobs Loudon, Esquire [klouden@mnat.com]
Morris Nichols Arsht & Tunnell
1201 North Market Street
PO Box 1347
Wilmington, DE 19899-1347

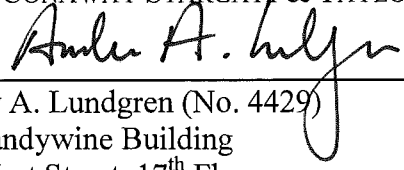
I further certify that on April 14, 2008, I caused a copy of the foregoing document to be served by hand delivery and e-mail on the above-listed counsel of record and on the following non-registered participants in the manner indicated:

BY E-MAIL

Behrooz Shariati, Esquire [bshariati@jonesday.com]
T. Gregory Lanier, Esquire [tglanier@jonesday.com]
Jones Day
1755 Embarcadero Road
Palo Alto, CA 94025

Kenneth R. Adamo [kradamo@jonesday.com]
Jones Day
2727 North Harwood Street
Dallas, TX 75201-1515

YOUNG CONAWAY STARGATT & TAYLOR, LLP


Andrew A. Lundgren (No. 4429)
The Brandywine Building
1000 West Street, 17th Floor
Wilmington, DE 19801
302-571-6600
alundgren@ycst.com